CR8F612X

16 MHz CR8F 8-bit MCU, up to 8 Kbytes Flash, 1 Kbyte RAM, 640 bytes EEPROM,10-bit ADC, 2 timers, UART, SPI, I²C

Preliminary data

Features

Core

- 16 MHz advanced CR8Fcore with Harvard architecture and 3-stage pipeline
- Extended instruction set

Memories

- Program memory: 8 Kbytes Flash; data retention 20 years at 55 °C after 10 kcycles
- Data memory: 640 bytes true data EEPROM; endurance 300 kcycles
- RAM: 1 Kbytes

Clock, reset and supply management

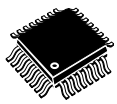
- 2.95 to 5.5 V operating voltage
- Flexible clock control, 4 master clock sources:
  - Low power crystal resonator oscillator
  - External clock input
  - Internal, user-trimmable 16 MHz RC
  - Internal low power 128 kHz RC
- Clock security system with clock monitor
- Power management:
  - Low power modes (wait, active-halt, halt)
  - Switch-off peripheral clocks individually
- Permanently active, low consumption power-on and power-down reset

Interrupt management

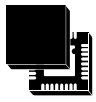
- Nested interrupt controller with 32 interrupts
- Up to 28 external interrupts on 7 vectors

Timers

- Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization



LQFP32 7x7



VFQFPN32 5x5

- 16-bit general purpose timer, with 3 CAPCOM channels (IC, OC or PWM)
- 8-bit basic timer with 8-bit prescaler
- Auto wake-up timer
- 2 watchdog timers: Window watchdog and independent watchdog

Communications interfaces

- UART with clock output for synchronous operation, Smartcard, IrDA, LIN master mode
- SPI interface up to 8 Mbit/s
- I^2C interface up to 400 Kbit/s

Analog to digital converter (ADC)

- 10-bit, ±1 LSB ADC with up to 7 multiplexed channels + 1 internal channel, scan mode and analog watchdog

I/Os

- Up to 28 I/Os on a 32-pin package including 21 high sink outputs
- Highly robust I/O design, immune against current injection
- Development support
  - Embedded single wire interface module (SWIM) for fast on-chip programming and non intrusive debugging

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1 Introduction

This datasheet contains the description of the CR8F612X features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the CR8F microcontroller memory, registers and peripherals, please refer to the CR8F microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the CR8F Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the CR8F SWIM communication protocol and debug module user manual (UM0470).
- For information on the CR8F core, please refer to the CR8F CPU programming manual (PM0044).

2 Description

The CR8F612X 8-bit microcontroller offers 8 Kbytes Flash program memory, plus integrated true data EEPROM. The CR8F microcontroller family reference manual (RM0016) refers to devices in this family as low-density. They provide the following benefits:

- Reduced system cost
  - Integrated true data EEPROM for up to 300 k write/erase cycles
  - High system integration level with internal clock oscillators, watchdog and brown-out reset
- Performance and robustness
  - 16 MHz CPU clock frequency
  - Robust I/O, independent watchdogs with separate clock source
  - Clock security system
- Full documentation and a wide choice of development tools
- Advanced core and peripherals made in a state-of-the art technology

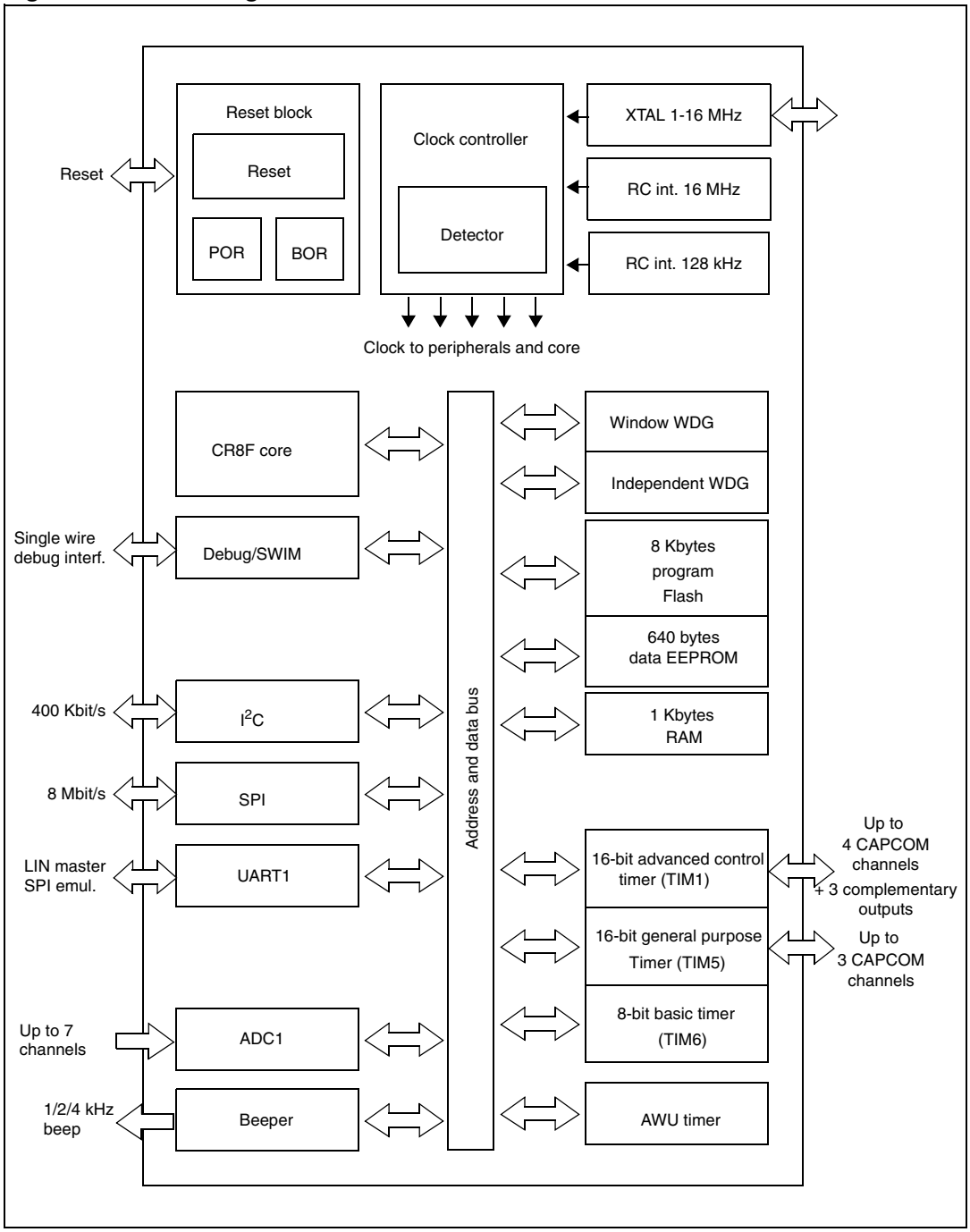
Table 1. CR8F612X access line features

Device	Pin count	No. of maximum GPIO (I/O)	Ext. interrupt pins	Timer CAPCOM channels	Timer complemetarty outputs	A/D converter channels	High sink I/Os	Low density Flash program memory (bytes)	Data EEPROM (bytes)	RAM (bytes)	Peripheral set
CR8F6126T	32	28	27	7	3	7	20	8K	640(1)	1K	Multipurpose timer (TIM1), SPI, I2C, UART window WDG, independent WDG, ADC PWM timer (TIM5) 8-bit timer (TIM6)
CR8F6125	28	24	24	7	3	7	20	8K	640(1)	1K	
CR8F6124	24	20	20	7	0	7	18	8K	640(1)	1K	
CR8F6123	20	16	16	7	0	3	12	8K	640(1)	1K	
CR8F6122	14	10	10	7	0	5	8	8K	640(1)	1K	

1. Including 21 high sink outputs
2. No read-while-write (RWW) capability

3 Block diagram

Figure 1. Block diagram



4 Product overview

The following section intends to give an overview of the basic features of the CR8F612X functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit CR8F

The 8-bit CR8F core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 28 external interrupts on 7 vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- 8 Kbytes of Flash program single voltage Flash memory
- 640 bytes true data EEPROM
- User option byte area

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to *Figure 2*.

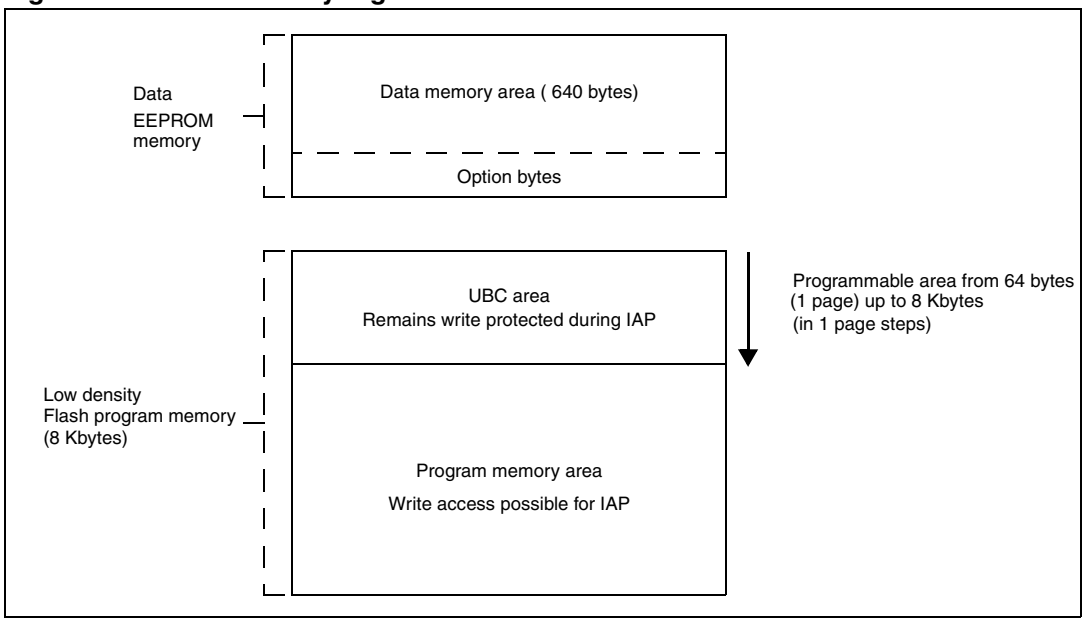
The size of the UBC is programmable through the UBC option byte (*Table 8*), in increments of 1 page (64-byte block) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 8 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 8 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organisation



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- ***Clock prescaler***: To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- ***Safe clock switching***: Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- ***Clock management***: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- ***Master clock sources***: Four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- ***Startup clock***: After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- ***Clock security system (CSS)***: This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- ***Configurable main clock output (CCO)***: This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART1	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	TIM5	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	Reserved	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM6	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

4.6 Power management

For efficent power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHZ LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM1 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals or to synchronize with TIM5 or TIM6
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM5 - 16-bit general purpose timer

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- 3 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM6

4.12 TIM6 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update
- Synchronization module to control the timer with external signals or to synchronize with TIM1 or TIM5

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchronization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	Yes
TIM5	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM6	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC1)

CR8F612X products contain a 10-bit successive approximation A/D converter (ADC1) with up to 7 external and 1 internal multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DD}
- Conversion time: 14 clock cycles
- Single and continuous and buffered continuous conversion modes
- Buffer size (n x 10 bits) where x = number of input channels
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Internal reference voltage on channel AIN7. This internal reference is constant and can be used for example, to monitor V_{DD}. It is independent of variations in V_{DD} and ambient temperature T_A.
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, synchronous mode, SPI master mode, Smartcard mode, IrDA mode, single wire mode, LIN2.1 master capability
- SPI : Full and half-duplex, 8 Mbit/s
- I²C: Up to 400 Kbit/s

4.14.1 UART1

Main features

- One Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: Generates 13-bit synch break frame
- Reception: Detects 11-bit break frame

4.14.2 SPI

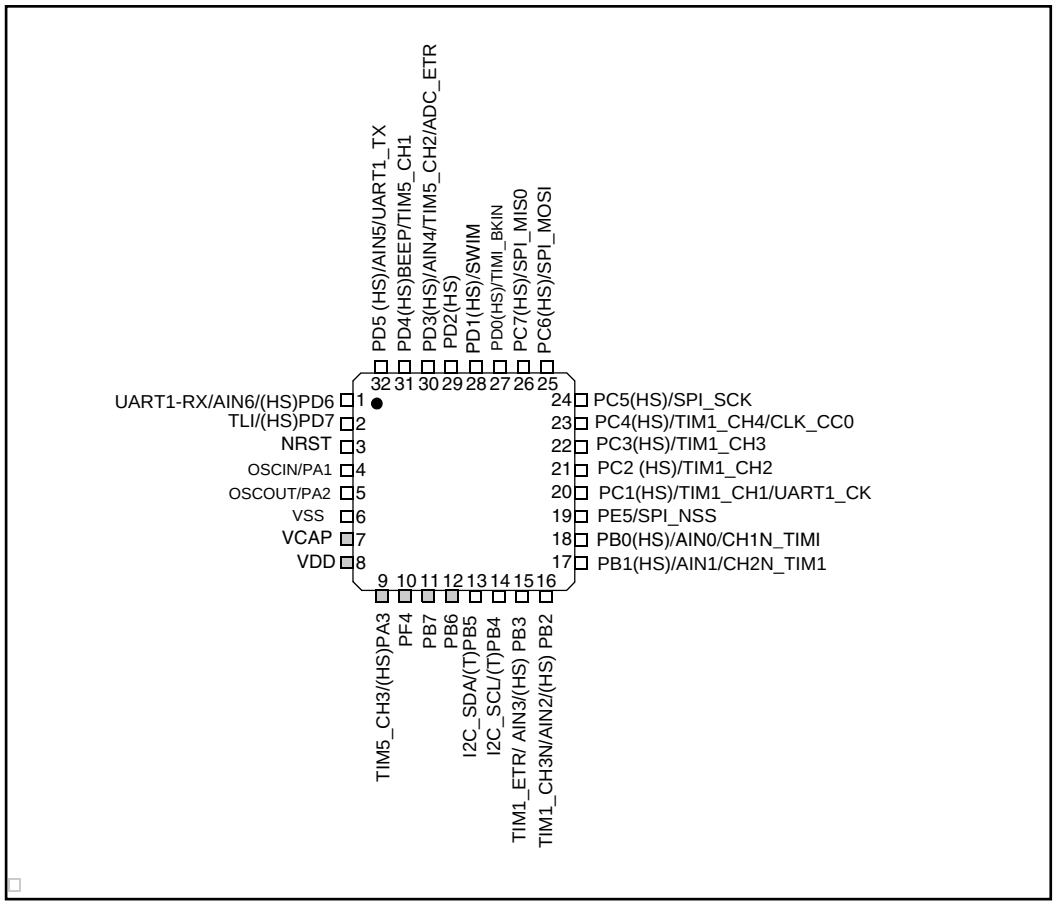
- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.3 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

5 Pinout and pin description

Figure 3. CR8F612X VFQFPN32/LQFP32 pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 4. Legend/abbreviations

Type	I= Input, O = Output, S = Power supply	
Level	Input	CM = CMOS
	Output	HS = High sink
Output speed	O1 = Slow (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = True open drain, OD = Open drain, PP = Push pull

Reset state is shown in **bold**.

Table 5. VFQFPN32/LQFP32 pin description

Pin no.	Pin name	Type	Input				Output			Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
1	PD6/AIN6/UART1_RX	I/O	**X**	X	X	HS	O3	X	X	**Port D6**	Analog input 6/ UART1 data receive	
2	PD7/TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	**Port D7**	Top level interrupt	Timer 1 - channel 4 [AFR6]
3	NRST	I/O		**X**						Reset		
4	PA1/OSCIN(2)	I/O	**X**	X	X		O1	X	X	**Port A1**	Resonator/crystal in	
5	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/crystal out	
6	V_{SS}	S								Digital ground		
7	VCAP	S								1.8 V regulator capacitor		
8	V_{DD}	S								Digital power supply		
9	PA3/TIM5_CH3 [SPI_NSS] [UART1_TX]	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 5 channel 3	SPI master/ slave select [AFR1]/ UART1 data transmit [AFR1:0]
10	PF4 [UART1_RX]	I/O	**X**	X			O1	X	X	**Port F4**		UART1 data receive [AFR1:0]

Table 5. VFQFPN32/LQFP32 pin description (continued)

Pin no.	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
11	PB7	I/O	**X**	X	X		O1	X	X	**Port B7**		
12	PB6	I/O	**X**	X	X		O1	X	X	**Port B6**		
13	PB5/I2C_SDA [TIM1_BKIN]	I/O	**X**	X	X		O1	T(3)	X	**Port B5**	I^2C data	Timer 1 - break input [AFR4]
14	PB4/I2C_SCL [ADC_ETR]	I/O	**X**	X	X		O1	T(3)	X	**Port B4**	I^2C clock	ADC external trigger [AFR4]
15	PB3/AIN3/TIM1_ETR	I/O	**X**	X	X	HS	O3	X	X	**Port B3**	Analog input 3/ Timer 1 external trigger	
16	PB2/AIN2/TIM1_CH3N	I/O	**X**	X	X	HS	O3	X	X	**Port B2**	Analog input 2/ Timer 1 - inverted channel 3	
17	PB1/AIN1/TIM1_CH2N	I/O	**X**	X	X	HS	O3	X	X	**Port B1**	Analog input 1/ Timer 1 - inverted channel 2	
18	PB0/AIN0/TIM1_CH1N	I/O	**X**	X	X	HS	O3	X	X	**Port B0**	Analog input 0/ Timer 1 - inverted channel 1	
19	PE5/SPI_NSS [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	**Port E5**	SPI master/slave select	Timer 1 - inverted channel 1 [AFR1:0]
20	PC1/TIM1_CH1/ UART1_CK [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1 UART1 clock	Timer 1 - inverted channel 2 [AFR1:0]

Table 5. VFQFPN32/LQFP32 pin description (continued)

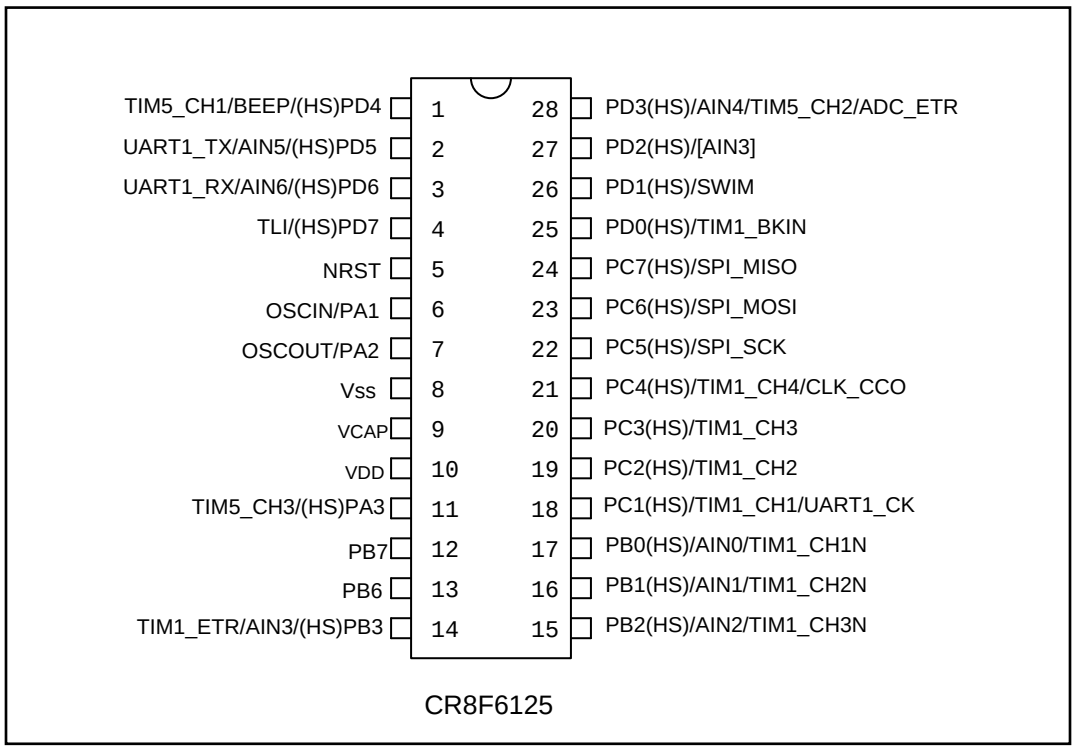
Pin no.	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
21	PC2/TIM1_CH2 [TIM1_CH3N]	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1 - channel 2	Timer 1 - inverted channel 3 [AFR1:0]
22	PC3/TIM1_CH3 [TLI] [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	Analog [AFR3] Timer 1 inverted channel 1 [AFR7]
23	PC4/TIM1_CH4/ CLK_CCO [AIN2] [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4 /configurable clock output	Analog input 2 [AFR2] Timer 1 inverted channel 2 [AFR7]
24	PC5/SPI_SCK [TIM5_CH1]	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	Timer 5 channel 1 [AFR0]
25	PC6/SPI_MOSI [TIM1_CH1]	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/ slave in	Timer 1 channel 1 [AFR0]
26	PC7/SPI_MISO [TIM1_CH2]	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	Timer 1 channel 2 [AFR0]
27	PD0/TIM1_BKIN [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 1 - break input	Con-figurable clock output [AFR5]
28	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
29	PD2 [AIN3] [TIM5_CH3]	I/O	**X**	X	X	HS	O3	X	X	**Port D2**		Analog input 3 [AFR2] Timer 5 - channel 3 [AFR1]
30	PD3/AIN4/TIM5_CH2/ ADC_ETR	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Analog input 4 Timer 5 - channel 2/ADC external trigger	

Table 5. VFQFPN32/LQFP32 pin description (continued)

Pin no.	Pin name	Type	Input				Output			Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
31	PD4/TIM5_CH1/BEEP [UART1_CK]	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 5 - channel 1/BEEP output	UART clock [AFR2]
32	PD5/AIN5/UART1_TX	I/O	**X**	X	X	HS	O3	X	X	**Port D5**	Analog input 5/ UART1 data transmit	

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings (see *Table 15: Current characteristics*.
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)

Figure 4 CR8F6125 28SOP/DIP



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 4 CR8F6124 SOP/DIP 24

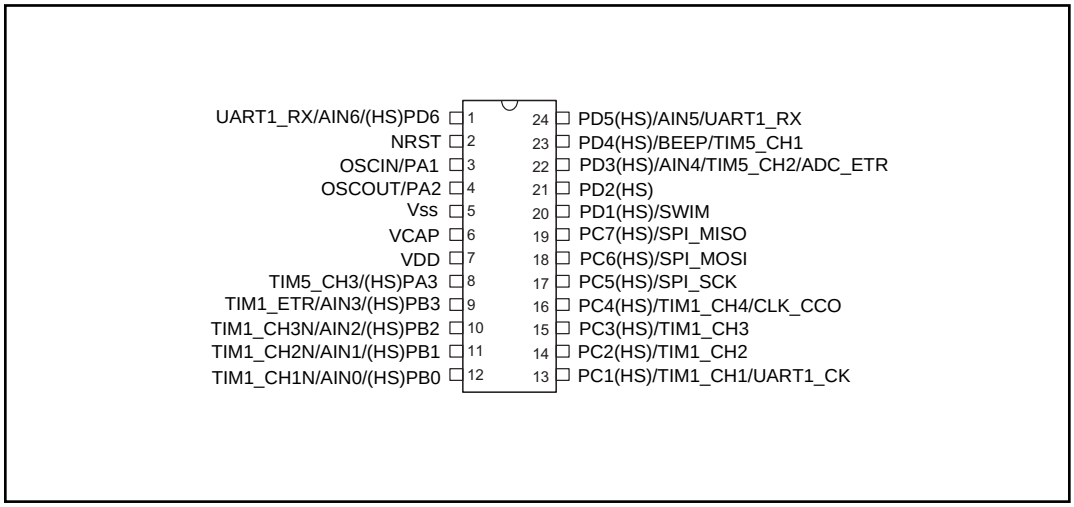
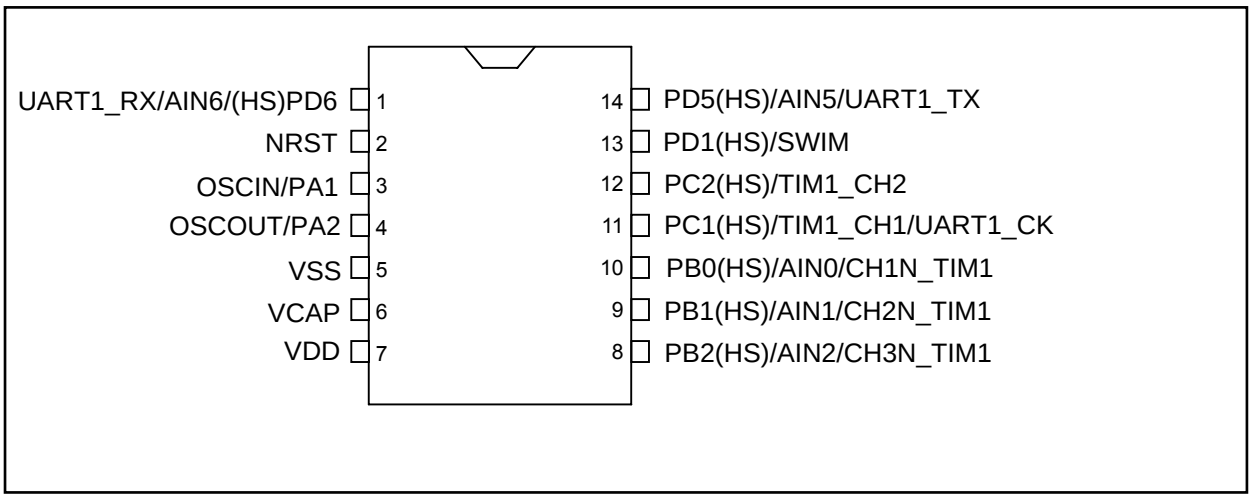
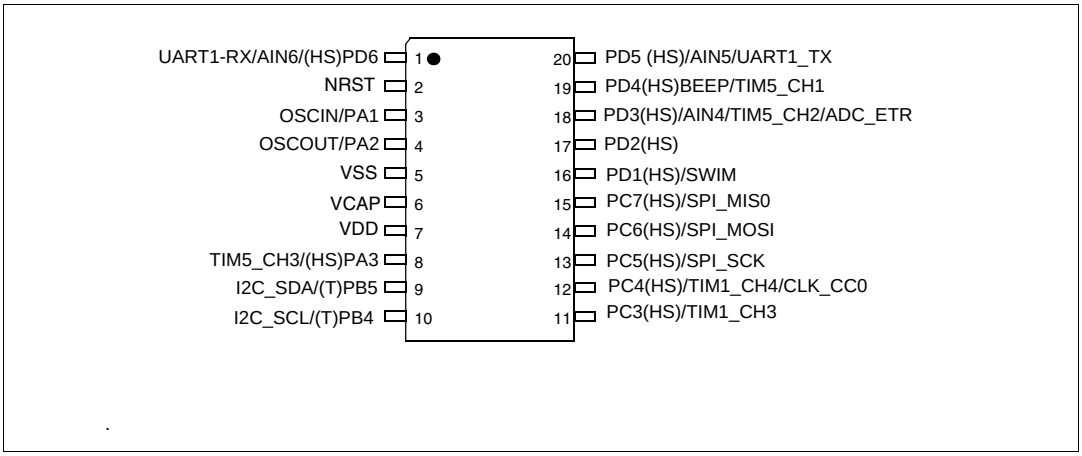


Figure6 CR8F6122B/M SOP/DIP 14



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Figure 7 CR8F6123 SOP 20



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

5.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 7: Option bytes*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

6 Interrupt vector mapping

Table 6. Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
	RESET	Reset	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level Interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8	EXTI5	Port F interrupt	Yes	Yes	0x00 8028
9		Reserved	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/overflow/underflow/ trigger/break	-	-	0x00 8034
12	TIM1	TIM1 capture/compare	-	-	0x00 8038
13	TIM5	TIM5 update /overflow/trigger	-	-	0x00 803C
14	TIM5	TIM5 capture/compare	-	-	0x00 8040
15		Reserved	-	-	0x00 8044
16		Reserved	-	-	0x00 8048
17	UART1	Tx complete	-	-	0x00 804C
18	UART1	Receive register DATA FULL	-	-	0x00 8050
19	I^2C	I^2C interrupt	Yes	Yes	0x00 8054
20		Reserved	-	-	0x00 8058
21		Reserved	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/analog watchdog interrupt	-	-	0x00 8060
23	TIM6	TIM6 update/overflow/trigger	-	-	0x00 8064
24	Flash	EOP/WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

1. Except PA1

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 7: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the CR8F Flash programming manual (PM0051) and CR8F SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 7. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
0x4801	User boot code(UBC)	OPT1	UBC[7:0]								00h
0x4802		NOPT1	NUBC[7:0]								FFh
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
0x4805h	Miscellaneous option	OPT3	Reserved			HSITRIM	LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	00h
0x4806		NOPT3	Reserved			NHSI-TRIM	NLSI_EN	NIWDG_HW	NWWDG_HW	NWWG_HALT	FFh
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	00h
0x4808		NOPT4	Reserved				NEXT CLK	NCKAWUSEL	NPR SC1	NPR SC0	FFh
0x4809	HSE clock startup	OPT5	HSECNT[7:0]								00h
0x480A		NOPT5	NHSECNT[7:0]								FFh

Table 8. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** *User boot code area* 0x00: no UBC, no write-protection 0x01: Page 0 defined as UBC, memory write-protected 0x02: Pages 0 to 1 defined as UBC, memory write-protected. Page 0 and 1 contain the interrupt vectors. ... 0x7F: Pages 0 to 126 defined as UBC, memory write-protected Other values: Pages 0 to 127 defined as UBC, memory write-protected *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	AFR[7:0] Refer to *Table 9* and *Table 10* for alternate function remapping decriptions of bits [7:2] and [1:0] respectively.
OPT3	**HSITRIM:** *High speed internal clock trimming register size* 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register
	LSI_EN: *Low speed internal clock enable* 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: *Independent watchdog* 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: *Window watchdog activation* 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: *Window watchdog reset on halt* 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active

Table 8. Option byte description (continued)

Option byte no.	Description
OPT4	**EXTCLK:** *External clock selection* 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: *Auto wake-up unit/clock* 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

Table 9. CR8F612X alternate function remapping bits [7:2]

Option byte no.	Description(1)
OPT2	**AFR7** *Alternate function remapping option 7* 0: AFR7 remapping option inactive: Default alternate functions(2). 1: Port C3 alternate function = TIM1_CH1N; port C4 alternate function = TIM1_CH2N. **AFR6** *Alternate function remapping option 6* 0: AFR6 remapping option inactive: Default alternate function(2). 1: Port D7 alternate function = TIM1_CH4. **AFR5** *Alternate function remapping option 5* 0: AFR5 remapping option inactive: Default alternate function(2). 1: Port D0 alternate function = CLK_CCO. **AFR4** *Alternate function remapping option 4* 0: AFR4 remapping option inactive: Default alternate functions(2). 1: Port B4 alternate function = ADC_ETR; port P5 alternate function = TIM1_BKIN. **AFR3** *Alternate function remapping option 3* 0: AFR3 remapping option inactive: Default alternate function(2). 1: Port C3 alternate function = TLI. **AFR2** *Alternate function remapping option 2* 0: AFR2 remapping option inactive: Default alternate functions(2). 1: Port C4 alternate function = AIN2; port D2 alternate function = AIN3; port D4 alternate function = UART1_CK.

1. Do not use more than one remapping option in the same port.
2. Refer to pinout description.

Table 10. CR8F612X alternate function remapping bits [1:0]

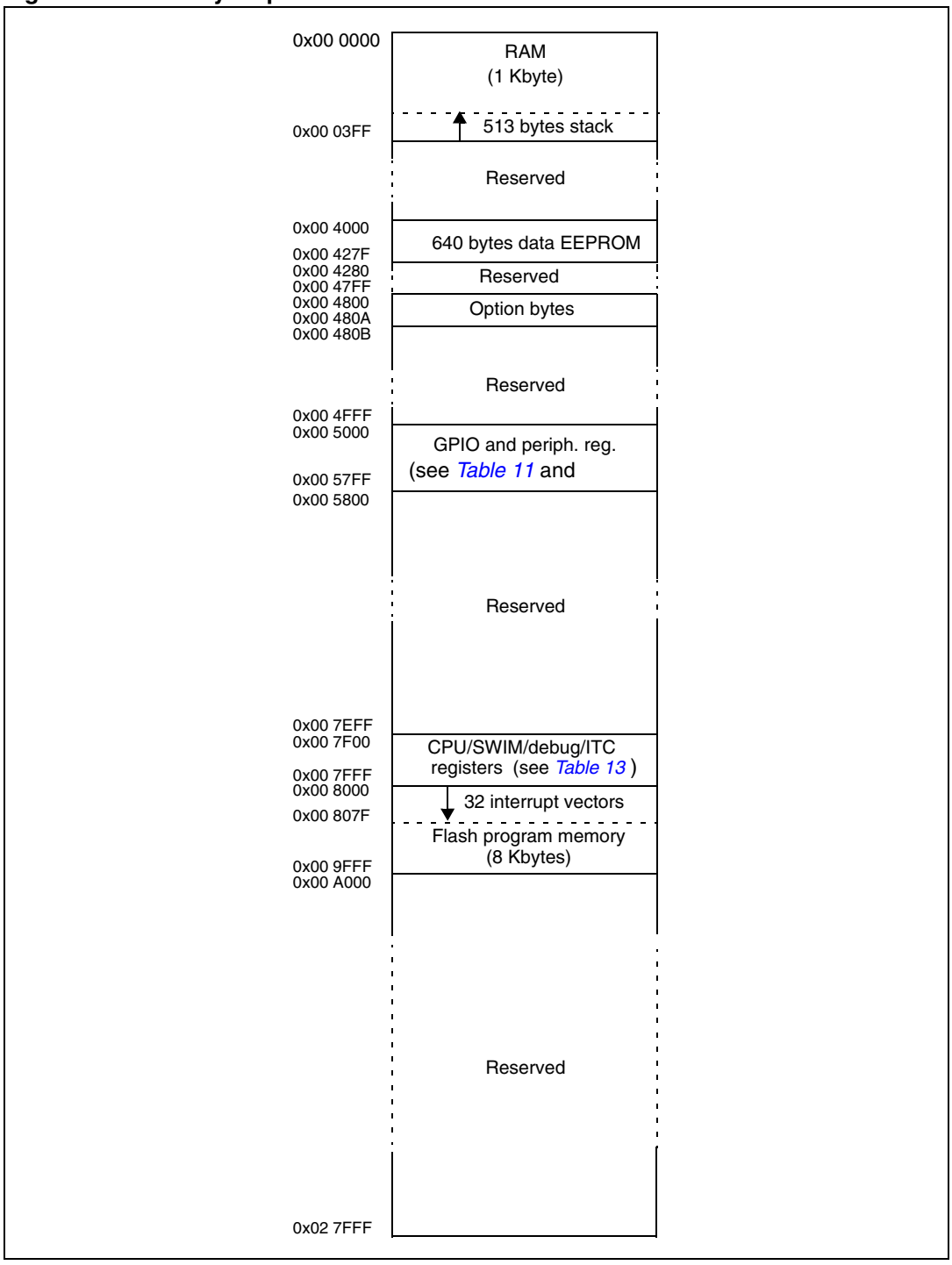
AFR1 option bit value	AFR0 option bit value	I/O port	Alternate function mapping
0	0	AFR1 and AFR0 remapping options inactive: Default alternate functions(1)	
0	1	PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
1	0	PA3	SPI_NSS
		PD2	TIM5_CH3
1	1	PD2	TIM5_CH3
		PC5	TIM5_CH1
		PC6	TIM1_CH1
		PC7	TIM1_CH2
		PC2	TIM1_CH3N
		PC1	TIM1_CH2N
		PE5	TIM1_CH1N
		PA3	UART1_TX
		PF4	UART1_RX

1. Refer to pinout description.

8 Memory and register map

8.1 Memory map

Figure 4. Memory map



8.2 Register map

Table 11. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0x00
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0x00
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0x00
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0x00
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x02
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0x00
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0x00
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00

Table 12. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 501E to 0x00 5059	Reserved area (60 bytes)			
0x00 505A	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 505B		FLASH_CR2	Flash control register 2	0x00
0x00 505C		FLASH_NCR2	Flash complementary control register 2	0xFF
0x00 505D		FLASH _FPR	Flash protection register	0x00
0x00 505E		FLASH _NFPR	Flash complementary protection register	0xFF
0x00 505F		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5060 to 0x00 5061	Reserved area (2 bytes)			
0x00 5062	Flash	FLASH _PUKR	Flash program memory unprotection register	0x00
0x00 5063	Reserved area (1 byte)			
0x00 5064	Flash	FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5065 to 0x00 509F	Reserved area (59 bytes)			
0x00 50A0	ITC	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2 to 0x00 50B2	Reserved area (17 bytes)			
0x00 50B3	RST	RST_SR	Reset status register	xx
0x00 50B4 to 0x00 50BF	Reserved area (12 bytes)			
0x00 50C0	CLK	CLK_ICKR	Internal clock control register	0x01
0x00 50C1		CLK_ECKR	External clock control register	0x00
0x00 50C2	Reserved area (1 byte)			

Table 12. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50C3	CLK	CLK_CMSR	Clock master status register	0xE1
0x00 50C4		CLK_SWR	Clock master switch register	0xE1
0x00 50C5		CLK_SWCR	Clock switch control register	0bxxxx 0000
0x00 50C6		CLK_CKDIVR	Clock divider register	0x18
0x00 50C7		CLK_PCKENR1	Peripheral clock gating register 1	0xFF
0x00 50C8		CLK_CSSR	Clock security system register	0x00
0x00 50C9		CLK_CCOR	Configurable clock control register	0x00
0x00 50CA		CLK_PCKENR2	Peripheral clock gating register 2	0xFF
0x00 50CB		CLK_CANCCR	CAN clock control register	0x00
0x00 50CC		CLK_HSITRIMR	HSI clock calibration trimming register	xx
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	x0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	-
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			

Table 12. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I^2C	I2C_CR1	I^2C control register 1	0x00
0x00 5211		I2C_CR2	I^2C control register 2	0x00
0x00 5212		I2C_FREQR	I^2C frequency register	0x00
0x00 5213		I2C_OARL	I^2C Own address register low	0x00
0x00 5214		I2C_OARH	I^2C Own address register high	0x00
0x00 5215		Reserved		
0x00 5216		I2C_DR	I^2C data register	0x00
0x00 5217		I2C_SR1	I^2C status register 1	0x00
0x00 5218		I2C_SR2	I^2C status register 2	0x00
0x00 5219		I2C_SR3	I^2C status register 3	0x0x
0x00 521A		I2C_ITR	I^2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I^2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I^2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I^2C TRISE register	0x02
0x00 521E		I2C_PECR	I^2C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 bytes)			

Table 12. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5230	UART1	UART1_SR	UART1 status register	C0h
0x00 5231		UART1_DR	UART1 data register	xxh
0x00 5232		UART1_BRR1	UART1 baud rate register 1	00h
0x00 5233		UART1_BRR2	UART1 baud rate register 2	00h
0x00 5234		UART1_CR1	UART1 control register 1	00h
0x00 5235		UART1_CR2	UART1 control register 2	00h
0x00 5236		UART1_CR3	UART1 control register 3	00h
0x00 5237		UART1_CR4	UART1 control register 4	00h
0x00 5238		UART1_CR5	UART1 control register 5	00h
0x00 5239		UART1_GTR	UART1 guard time register	00h
0x00 523A		UART1_PSCR	UART1 prescaler register	00h
0x00 523B to 0x00 523F	Reserved area (21 bytes)			
0x00 5250	TIM1	TIM1_CR1	TIM1 control register 1	0x00
0x00 5251		TIM1_CR2	TIM1 control register 2	0x00
0x00 5252		TIM1_SMCR	TIM1 slave mode control register	0x00
0x00 5253		TIM1_ETR	TIM1 external trigger register	0x00
0x00 5254		TIM1_IER	TIM1 interrupt enable register	0x00
0x00 5255		TIM1_SR1	TIM1 status register 1	0x00
0x00 5256		TIM1_SR2	TIM1 status register 2	0x00
0x00 5257		TIM1_EGR	TIM1 event generation register	0x00
0x00 5258		TIM1_CCMR1	TIM1 capture/compare mode register 1	0x00
0x00 5259		TIM1_CCMR2	TIM1 capture/compare mode register 2	0x00
0x00 525A		TIM1_CCMR3	TIM1 capture/compare mode register 3	0x00
0x00 525B		TIM1_CCMR4	TIM1 capture/compare mode register 4	0x00
0x00 525C		TIM1_CCER1	TIM1 capture/compare enable register 1	0x00
0x00 525D		TIM1_CCER2	TIM1 capture/compare enable register 2	0x00
0x00 525E		TIM1_CNTRH	TIM1 counter high	0x00

Table 12. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 525F	TIM1 cont'd	TIM1_CNTRL	TIM1 counter low	0x00
0x00 5260		TIM1_PSCRH	TIM1 prescaler register high	0x00
0x00 5261		TIM1_PSCRL	TIM1 prescaler register low	0x00
0x00 5262		TIM1_ARRH	TIM1 auto-reload register high	0xFF
0x00 5263		TIM1_ARRL	TIM1 auto-reload register low	0xFF
0x00 5264		TIM1_RCR	TIM1 repetition counter register	0x00
0x00 5265		TIM1_CCR1H	TIM1 capture/compare register 1 high	0x00
0x00 5266		TIM1_CCR1L	TIM1 capture/compare register 1 low	0x00
0x00 5267		TIM1_CCR2H	TIM1 capture/compare register 2 high	0x00
0x00 5268		TIM1_CCR2L	TIM1 capture/compare register 2 low	0x00
0x00 5269		TIM1_CCR3H	TIM1 capture/compare register 3 high	0x00
0x00 526A		TIM1_CCR3L	TIM1 capture/compare register 3 low	0x00
0x00 526B		TIM1_CCR4H	TIM1 capture/compare register 4 high	0x00
0x00 526C		TIM1_CCR4L	TIM1 capture/compare register 4 low	0x00
0x00 526D		TIM1_BKR	TIM1 break register	0x00
0x00 526E		TIM1_DTR	TIM1 dead-time register	0x00
0x00 526F		TIM1_OISR	TIM1 output idle state register	0x00
0x00 5270 to 0x00 52FF	Reserved area (147 bytes)			
0x00 5300	TIM5	TIM5_CR1	TIM5 control register 1	0x00
0x00 5301		TIM5_CR2	TIM5 control register 2	0x00
0x00 5302		TIM5_SMCR	TIM5 slave mode control register	0x00
0x00 5303		TIM5_IER	TIM5 interrupt enable register	0x00
0x00 5304		TIM5_SR1	TIM5 status register 1	0x00
0x00 5305		TIM5_SR2	TIM5 status register 2	0x00
0x00 5306		TIM5_EGR	TIM5 event generation register	0x00
0x00 5307		TIM5_CCMR1	TIM5 capture/compare mode register 1	0x00
0x00 5308		TIM5_CCMR2	TIM5 capture/compare mode register 2	0x00
0x00 5309		TIM5_CCMR3	TIM5 capture/compare mode register 3	0x00
0x00 530A		TIM5_CCER1	TIM5 capture/compare enable register 1	0x00
0x00 530B		TIM5_CCER2	TIM5 capture/compare enable register 2	0x00

Table 12. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 530C0x	TIM5 cont'd	TIM5_CNTRH	TIM5 counter high	0x00
0x00 530D		TIM5_CNTRL	TIM5 counter low	0x00
0x00 530E		TIM5_PSCR	TIM5 prescaler register	0x00
0x00 530F		TIM5_ARRH	TIM5 auto-reload register high	0xFF
0x00 5310		TIM5_ARRL	TIM5 auto-reload register low	0xFF
0x00 5311		TIM5_CCR1H	TIM5 capture/compare register 1 high	0x00
0x00 5312		TIM5_CCR1L	TIM5 capture/compare register 1 low	0x00
0x00 5313		TIM5_CCR2H	TIM5 capture/compare register 2 high	0x00
0x00 5314		TIM5_CCR2L	TIM5 capture/compare register 2 low	0x00
0x00 5315		TIM5_CCR3H	TIM5 capture/compare register 3 high	0x00
0x00 5316		TIM5_CCR3L	TIM5 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 bytes)			
0x00 5340	TIM6	TIM6_CR1	TIM6 control register 1	0x00
0x00 5341		TIM6_CR2	TIM6 control register 2	0x00
0x00 5342		TIM6_SMCR	TIM6 slave mode control register	0x00
0x00 5343		TIM6_IER	TIM6 interrupt enable register	0x00
0x00 5344		TIM6_SR	TIM6 status register	0x00
0x00 5345		TIM6_EGR	TIM6 event generation register	0x00
0x00 5346		TIM6_CNTR	TIM6 counter	0x00
0x00 5347		TIM6_PSCR	TIM6 prescaler register	0x00
0x00 5348		TIM6_ARR	TIM6 auto-reload register	0xFF
0x00 5349 to 0x00 53DF	Reserved area (153 bytes)			
0x00 53E0 to 0x00 53F3	ADC1	ADC _DBxR	ADC data buffer registers	0x00
0x00 53F4 to 0x00 53FF	Reserved area (12 bytes)			

Table 12. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	ADC1 cont'd	ADC _CSR	ADC control/status register	0x00
0x00 5401		ADC_CR1	ADC configuration register 1	0x00
0x00 5402		ADC_CR2	ADC configuration register 2	0x00
0x00 5403		ADC_CR3	ADC configuration register 3	0x00
0x00 5404		ADC_DRH	ADC data register high	0x00
0x00 5405		ADC_DRL	ADC data register low	0x00
0x00 5406		ADC_TDRH	ADC Schmitt trigger disable register high	0x00
0x00 5407		ADC_TDRL	ADC Schmitt trigger disable register low	0x00
0x00 5408		ADC_HTRH	ADC high threshold register high	0x03
0x00 5409		ADC_HTRL	ADC high threshold register low	0xFF
0x00 540A		ADC_LTRH	ADC low threshold register high	0x00
0x00 540B		ADC_LTRL	ADC low threshold register low	0x00
0x00 540C		ADC_AWSRH	ADC analog watchdog status register high	0x00
0x00 540D		ADC_AWSRL	ADC analog watchdog status register low	0x00
0x00 540E		ADC _AWCRH	ADC analog watchdog control register high	0x00
0x00 540F	ADC1 cont'd	ADC_AWCRL	ADC analog watchdog control register low	0x00
0x00 5410 to 0x00 57FF	Reserved area (1008 bytes)			

Table 13. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			

Table 13. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM debug module control register 1	0x00
0x00 7F97		DM_CR2	DM debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

9 Electrical characteristics

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2 Σ).

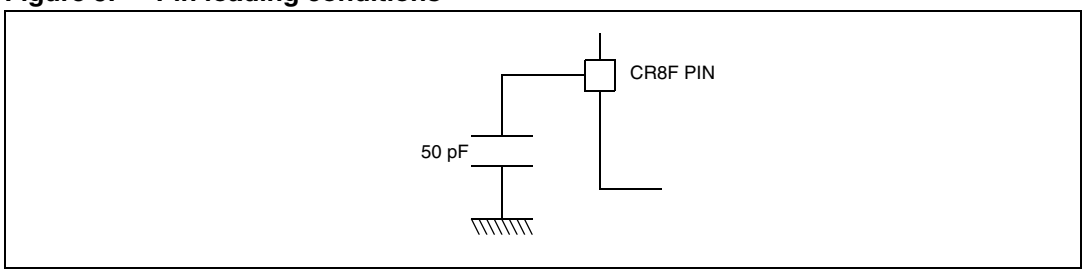
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 5*.

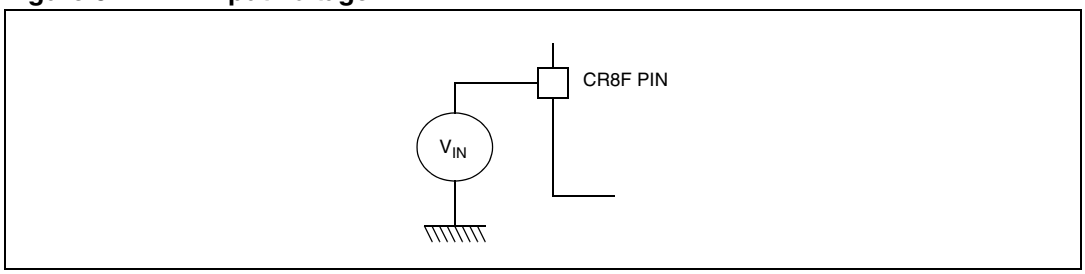
Figure 5. Pin loading conditions



9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 6*.

Figure 6. Pin input voltage



9.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins		50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 76*		

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 15. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	- 20	
$I_{INJ(PIN)}$(3)(4)	Injected current on NRST pin	± 4	
	Injected current on OSCIN pin	± 4	
	Injected current on any other pin(5)	± 4	
$\Sigma I_{INJ(PIN)}$(3)	Total injected current (sum of all I/O and control pins)(5)	± 20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
4. Negative injection disturbs the analog performance of the device. See note in *Section 9.3.10: 10-bit ADC characteristics on page 72*.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

9.3 Operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency		0	16	MHz
V_{DD}	Standard operating voltage		2.95	5.5	V
C_{EXT}	VCAP external capacitor(1)	0.05 ≤ESR ≤ 0.2 Ω at 1 MHz	470	3300	nF
P_D(2)	Power dissipation at T_A = 85° C for suffix 6	LQFP32		330	mW
		VFQFPN32		550	
	Power dissipation at T_A = 125° C for suffix 3	LQFP32		83	
		VFQFPN32		110	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
	Ambient temperature for 3 suffix version	Maximum power dissipation	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	
		3 suffix version	-40	130(3)	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as its dependency on temperature, DC bias and frequency in addition to other factors
2. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *Section 10.2: Thermal characteristics*) with the value for T_{Jmax} given in *Table 17* and the value for Θ_{JA} given in *Table 52: Thermal characteristics*.
3. T_{Jmax} is given by the test limit. Above this value the product behavior is not guaranteed.

Figure 7. f_{CPUmax} versus V_{DD}

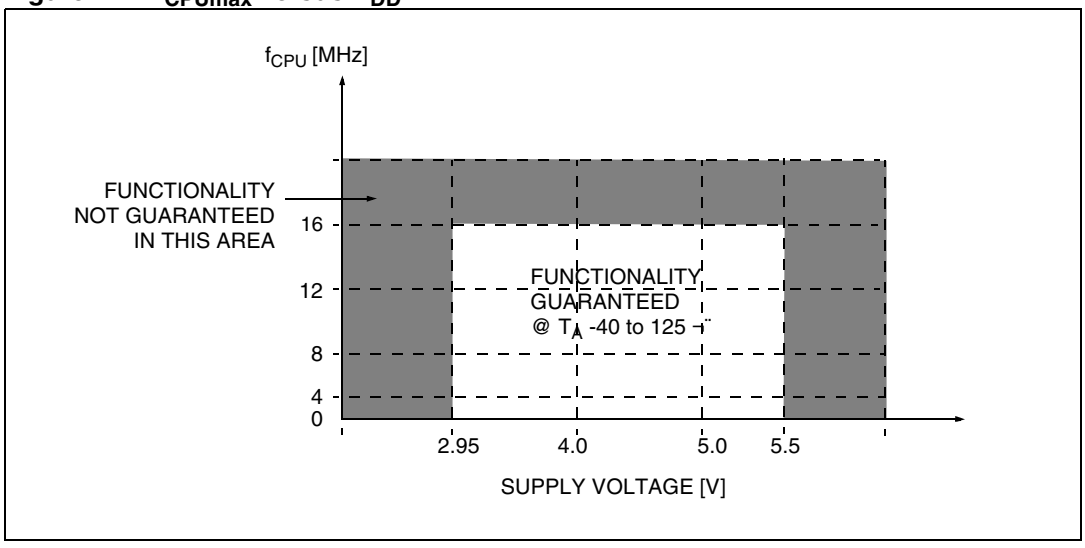


Table 18. Operating conditions at power-up/power-down

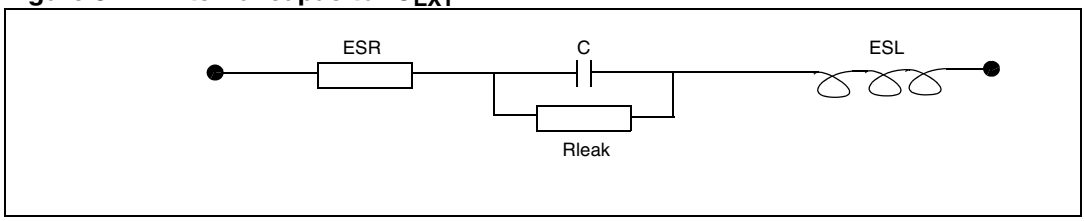
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		2		∞	µs/V
	V_{DD} fall time rate(1)		2		∞	
t_{TEMP}	Reset release delay	V_{DD} rising			1.7	ms
V_{IT+}	Power-on reset threshold		2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold		2.5	2.65	2.8	
$V_{HYS(BOR)}$	Brown-out reset hysteresis			70		mV

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum ooperating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 17*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 8. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 6 on page 42*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by peripheral clock gating registers) except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Table 19. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.3		mA
			HSE user ext. clock (16 MHz)	2	2.35	
			HSI RC osc. (16 MHz)	1.7	2	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	0.86		
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4.5		
			HSE user ext. clock (16 MHz)	4.3	4.75	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 20. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.8		mA
			HSE user ext. clock (16 MHz)	2	2.3	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	0.81		
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4		
			HSE user ext. clock (16 MHz)	3.9	4.7	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in wait mode

Table 21. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.6		mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 22. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max (1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.1		mA
			HSE user ext. clock (16 MHz)	1.1	1.3	
			HSI RC osc. (16 MHz)	0.89	1.1	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.7	0.88	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.45	0.57	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.4	0.54	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 23. Total current consumption in active halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 125 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	1030			µA
				LSI RC osc. (128 kHz)	200	260	300	
			Power-down mode	HSE crystal osc. (16 MHz)	970			
				LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	85	110	
			Power-down mode		10	20	40	

1. Data based on characterization results, not tested in production
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 24. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85 °C(1)	Max at 125 °C(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source				
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	550			µA
				LSI RC osc. (128 kHz)	200	260	290	
			Power-down mode	HSE crystal osc. (16 MHz)	970			
				LSI RC osc. (128 kHz)	150	200	230	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	80	105	
			Power-down mode		10	18	35	

1. Data based on characterization results, not tested in production
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Total current consumption in halt mode

Table 25. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 125 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	105	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	15	35	

1. Data based on characterization results, not tested in production

Table 26. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85 °C(1)	Max at 125 °C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	100	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	12	30	

1. Data based on characterization results, not tested in production

Low power mode wakeup times

Table 27. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(3)					See note(2)	µs
		$f_{CPU} = f_{MASTER}$ = 16 MHz.			0.56		
$t_{WU(AH)}$	Wakeup time active halt mode to run mode(3)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
			Flash in power-down mode(5)		3(6)		
		MVR voltage regulator off(4)	Flash in operating mode(5)		48(6)		
			Flash in power-down mode(5)		50(6)		
$t_{WU(H)}$	Wakeup time from halt mode to run mode(3)	Flash in operating mode(5)			52		
		Flash in power-down mode(5)			54		

1. Data guaranteed by design, not tested in production.
2. $t_{WU(WFI)} = 2 \times 1/f_{master} + 6 \times 1/f_{CPU}$.
3. Measured from interrupt event to interrupt vector fetch.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

Total current consumption and timing in forced reset state

Table 28. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	400		µA
		V_{DD} = 3.3 V	300		
$t_{RESETBL}$	Reset pin release to vector fetch			150	µs

1. Data guaranteed by design, not tested in production.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, V_{DD} = 5 V

Table 29. Peripheral current consumption

Symbol	Parameter	Typ.	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)	210	µA
$I_{DD(TIM5)}$	TIM5 supply current(1)	130	
$I_{DD(TIM6)}$	TIM6 timer supply current(1)	50	
$I_{DD(UART1)}$	UART1 supply current(2)	120	
$I_{DD(SPI)}$	SPI supply current(2)	45	
$I_{DD(I^2C)}$	I^2C supply current(2)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(3)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. No I/O pads toggling. Not tested in production.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions. Not tested in production.

Current consumption curves

Figure 9 to *Figure 14* show typical current consumption measured with code executing in RAM.

Figure 9. Typ $I_{DD(RUN)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

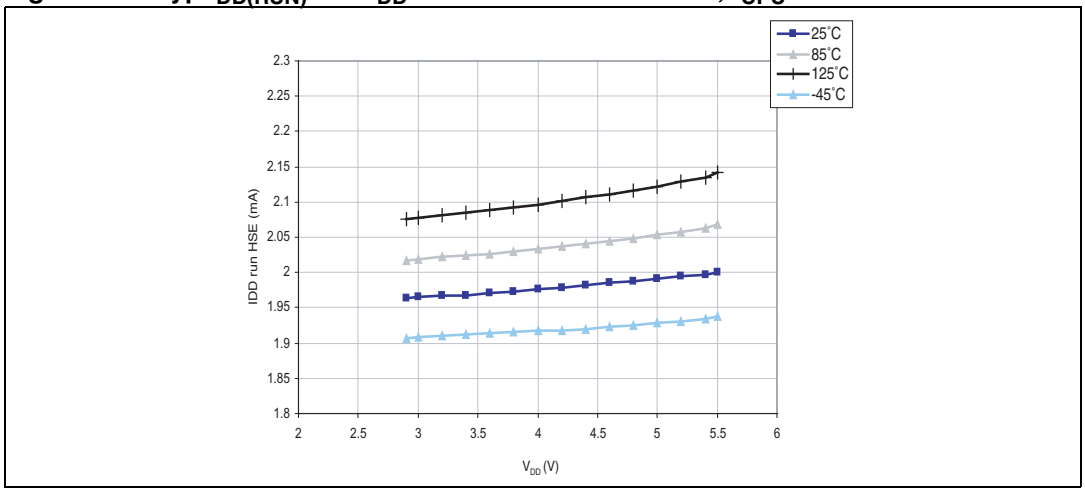


Figure 10. Typ $I_{DD(RUN)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V

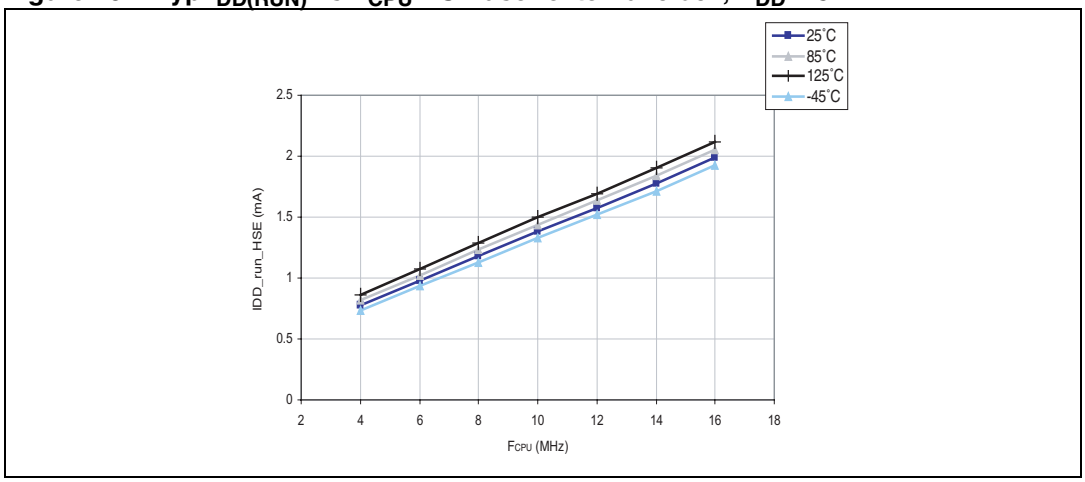


Figure 11. Typ $I_{DD(RUN)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz

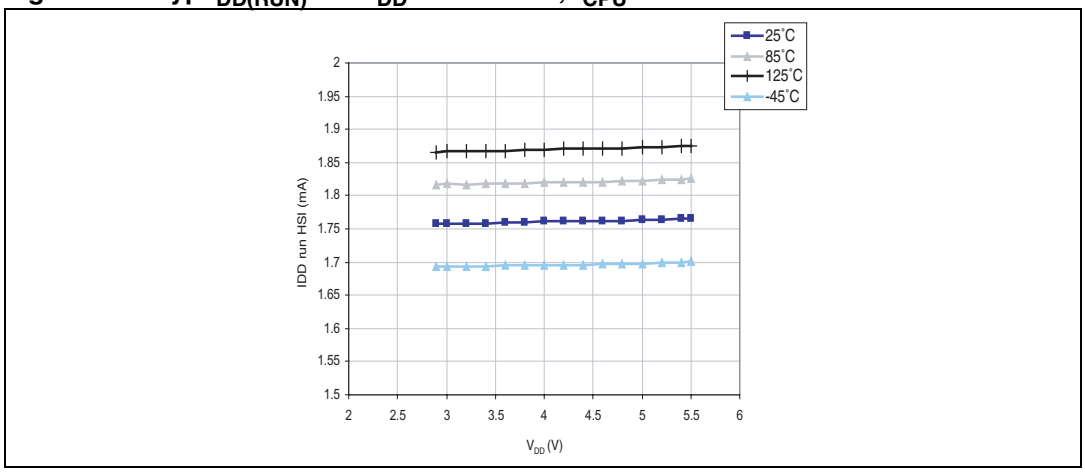


Figure 12. Typ $I_{DD(WFI)}$ vs. V_{DD} HSE user external clock, f_{CPU} = 16 MHz

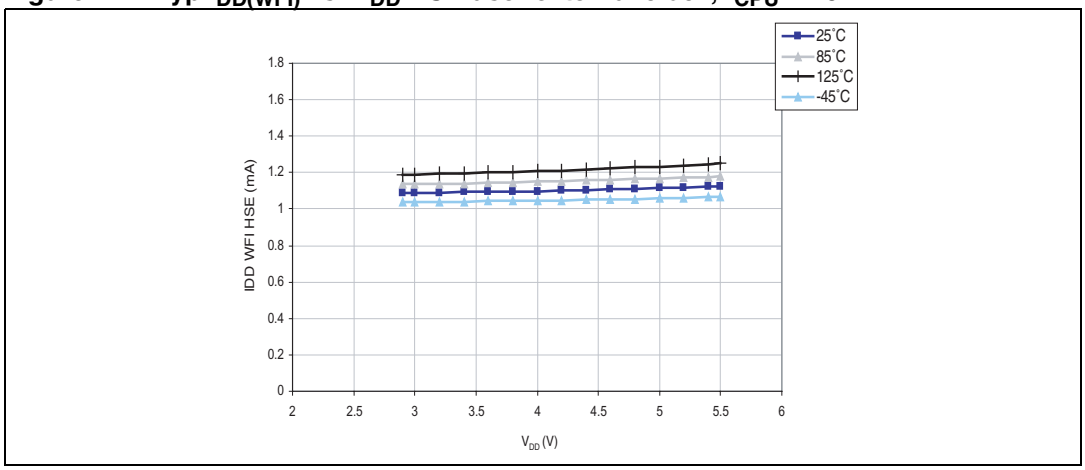


Figure 13. Typ $I_{DD(WFI)}$ vs. f_{CPU} HSE user external clock, V_{DD} = 5 V

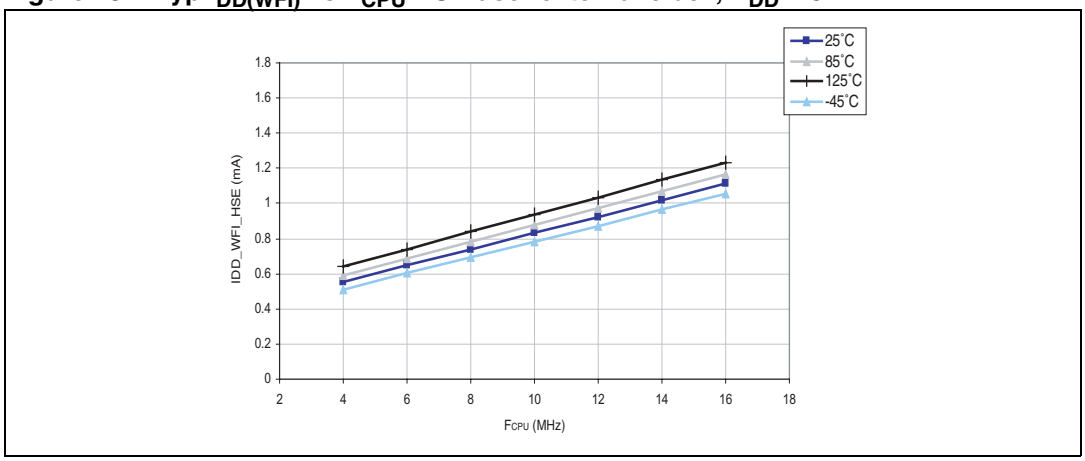
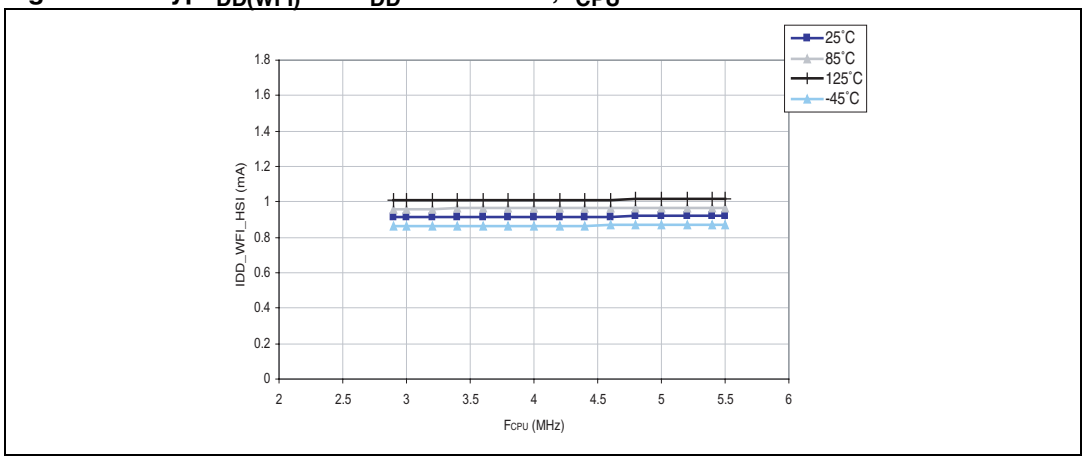


Figure 14. Typ $I_{DD(WFI)}$ vs. V_{DD} HSI RC osc, f_{CPU} = 16 MHz



9.3.3 External clock sources and timing characteristics

HSE user external clock

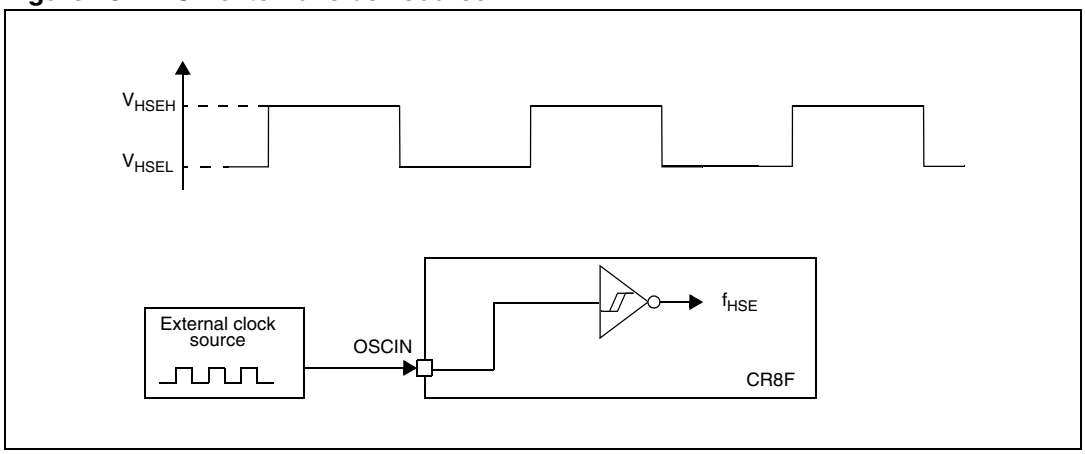
Subject to general operating conditions for V_{DD} and T_A.

Table 30. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HSE_ext}	User external clock source frequency		0	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage		0.7 x V_{DD}	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage		V_{SS}	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	+1	µA

1. Data based on characterization results, not tested in production.

Figure 15. HSE external clock source



HSE crystal/ceramic resonator oscillator

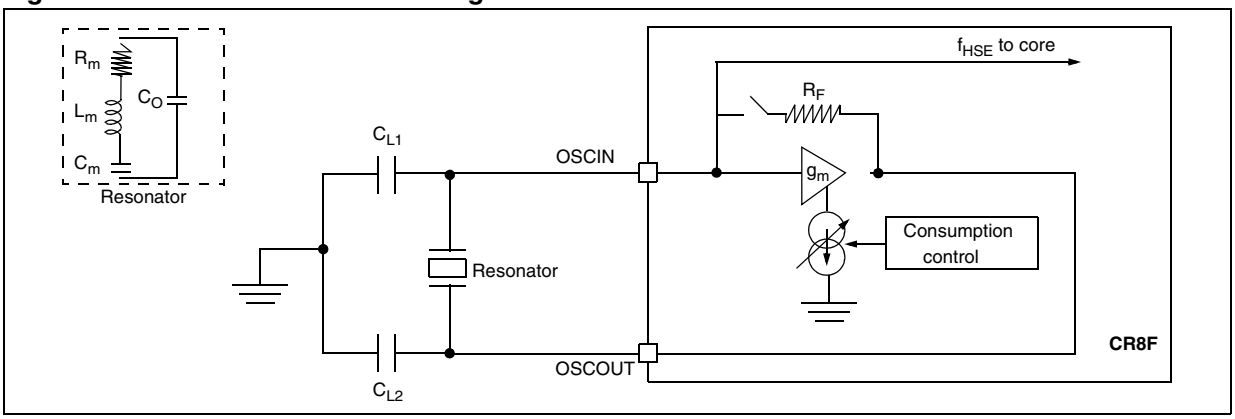
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency		1		16	MHz
R_F	Feedback resistor			220		kΩ
C(1)	Recommended load capacitance (2)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz			6 (startup) 1.6 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz			6 (startup) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 16. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
g_m >> g_{mcrit}

9.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator (HSI)

Table 32. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator	User-trimmed with CLK_HSITRIMR register for given V_{DD} and T_A conditions(1)			1(4)	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25°C(2)	-2.5(3)		1.3(3)	%
		V_{DD} = 5 V, 25 °C ≤T_A ≤85 °C	-2.5(3)		2(3)	%
		2.95 ≤ V_{DD} ≤ 5.5 V, -40 °C ≤T_A ≤125 °C	-4.5(2)(3)		3(2)(3)	%
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration				1(4)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			170	250(2)	µA

1. Refer to application note.
2. Data based on characterization results, not tested in production
3. Subject to further characterization to give better results
4. Guaranteeed by design, not tested in production.

Figure 17. Typical HSI accuracy at V_{DD} = 5 V vs 5 temperatures

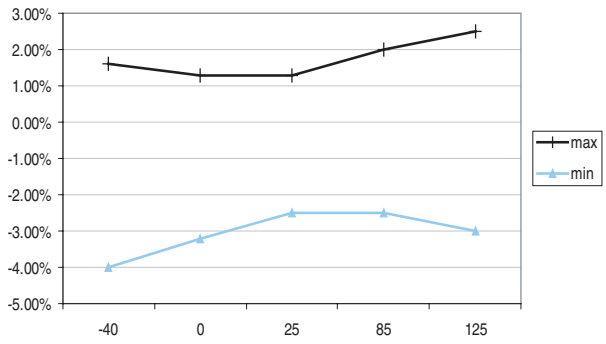
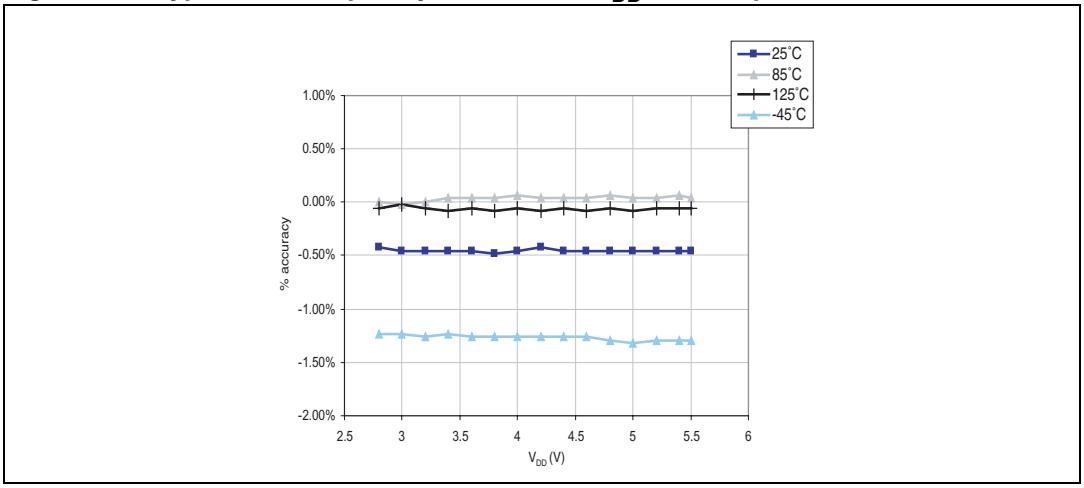


Figure 18. Typical HSI frequency variation vs V_{DD} @ 4 temperatures



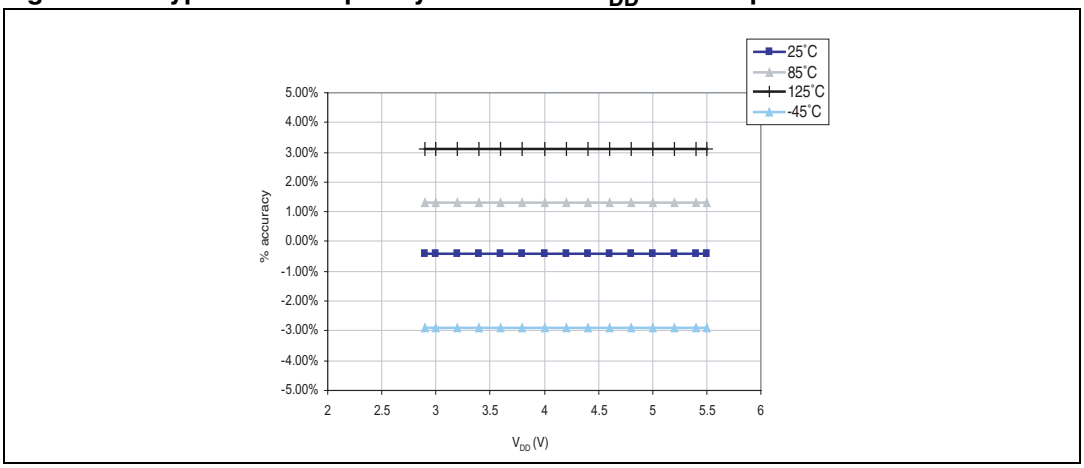
Low speed internal RC oscillator (LSI)

Subject to general operating conditions for V_{DD} and T_A.

Table 33. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		110	128	150	kHz
$t_{su(LSI)}$	LSI oscillator wake-up time				7	µs
$I_{DD(LSI)}$	LSI oscillator power consumption			5		µA

Figure 19. Typical LSI frequency variation vs V_{DD} @ 4 temperatures



9.3.5 Memory characteristics

RAM and hardware registers

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	2.8 V(2)			V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production.
2. Refer to *Table 18 on page 45* for the value of V_{IT-max}

Flash program memory/data EEPROM memory

Table 35. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	$f_{CPU} \leq 16$ MHz	2.95		5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/64 bytes)			6	6.6	ms
	Fast programming time for 1 block (64 bytes)			3	3.33	
t_{erase}	Erase time for 1 block (64 bytes)			3	3.33	
N_{RW}	Erase/write cycles(2) (program memory)	T_A = +85 °C	10 k			cycles
	Erase/write cycles (data memory)(2)	T_A = +125 °C	300 k	1 M		
t_{RET}	Data retention (program and data memory) after 10k erase/write cycles at T_A = +55 °C	T_{RET} = 55°C	20			years
	Data retention (data memory) after 300k erase/write cycles at T_A = +125 °C	T_{RET} = 85°C	1			
I_{DD}	Supply current (Flash programming or erasing for 1 to 128 bytes)			2		mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 36. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3 V		0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(1)			700		mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	45	60	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF			20	ns
		Standard and high sink I/Os Load = 50 pF			125	ns
I_{lkg}	Digital input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±250	
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA			±1	

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

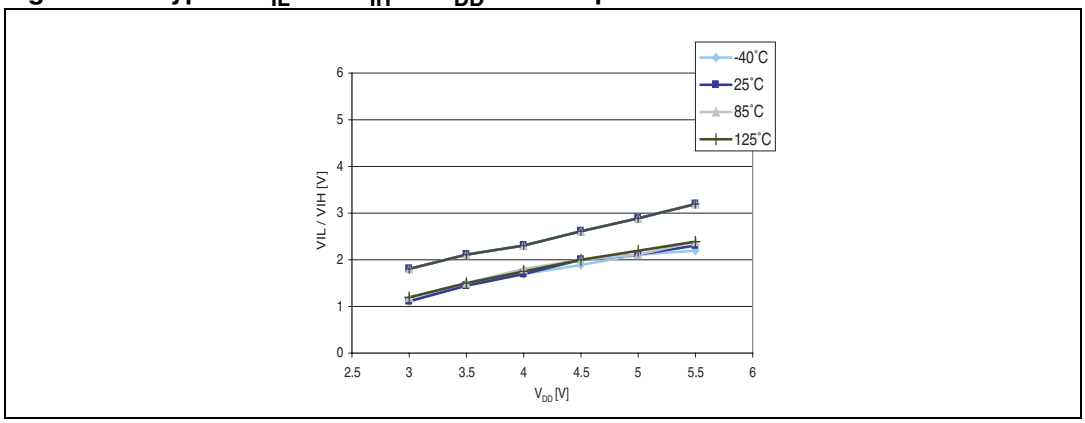


Figure 21. Typical pull-up resistance vs V_{DD} @ 4 temperatures

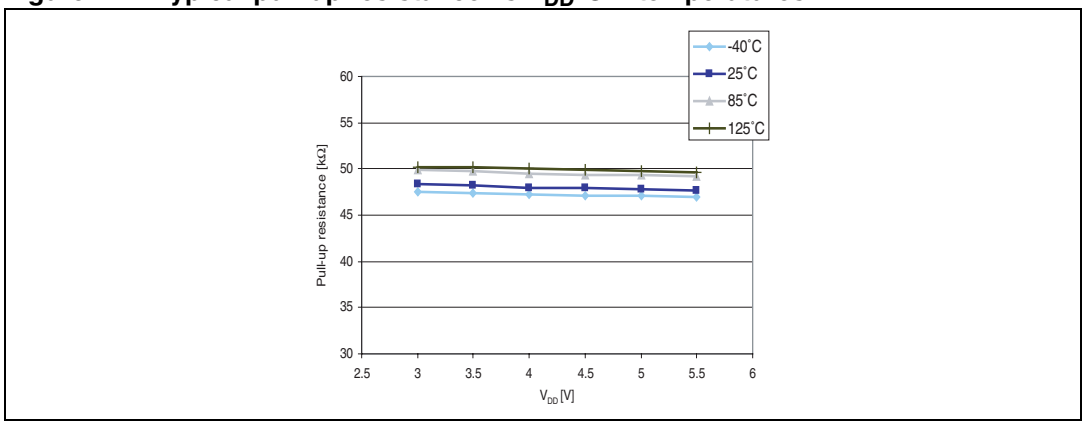


Figure 22. Typical pull-up current vs V_{DD} @ 4 temperatures

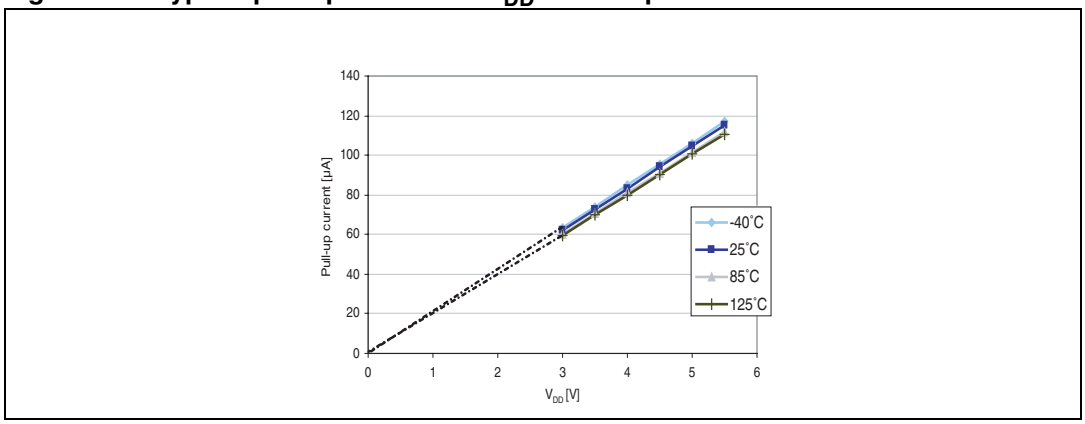


Table 37. Output driving current (standard ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 4 pins sunk	I_{IO} = 4 mA, V_{DD} = 3.3 V		1(1)	V
	Output low level with 8 pins sunk	I_{IO}= 10 mA, V_{DD} = 5 V		2	
V_{OH}	Output high level with 4 pins sourced	I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)		
	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	2.8		

1. Data based on characterization results, not tested in production

Table 38. Output driving current (true open drain ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 2 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V		1.5(1)	V
		I_{IO} = 10 mA, V_{DD} = 5 V		1	
		I_{IO} = 20 mA, V_{DD} = 5 V		2(1)	

1. Data based on characterization results, not tested in production

Table 39. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V		1(1)	V
	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V		0.8	
	Output low level with 4 pins sunk	I_{IO} = 20 mA, V_{DD} = 5 V		1.5(1)	
V_{OH}	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)		
	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0		
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)		

1. Data based on characterization results, not tested in production

Figure 23. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

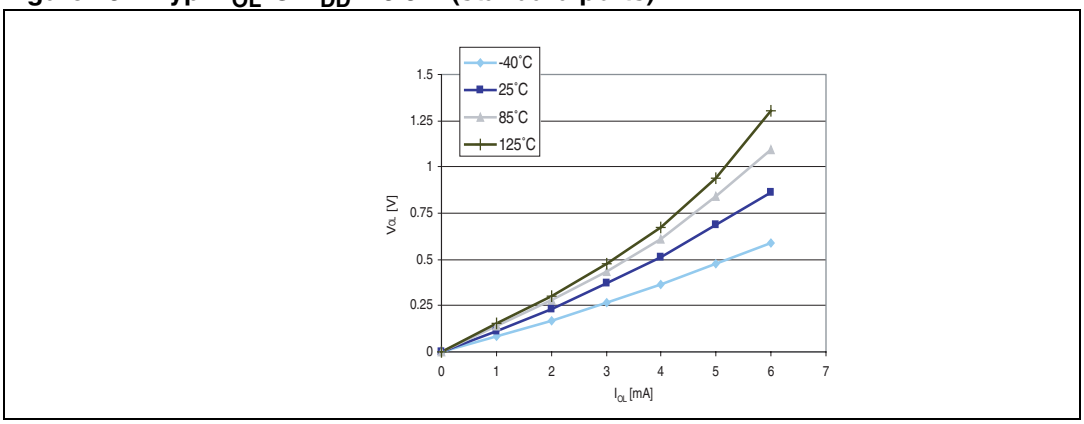


Figure 24. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

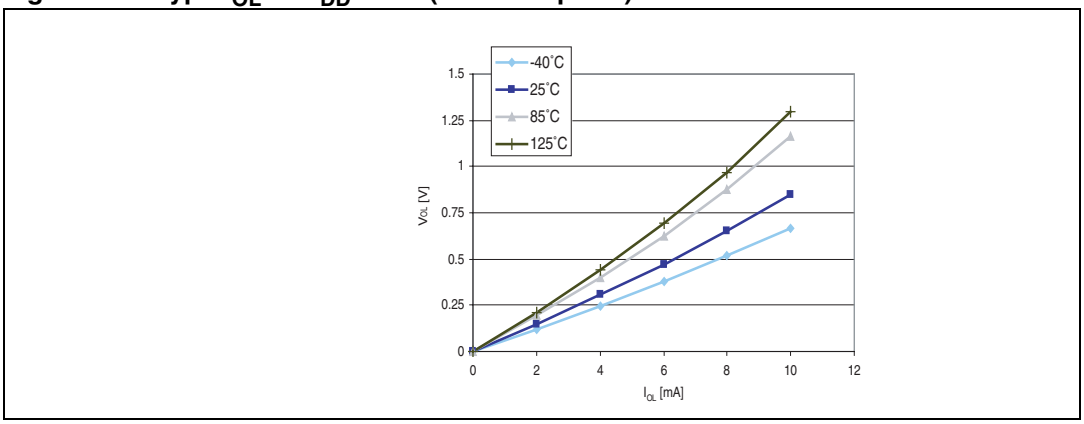


Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

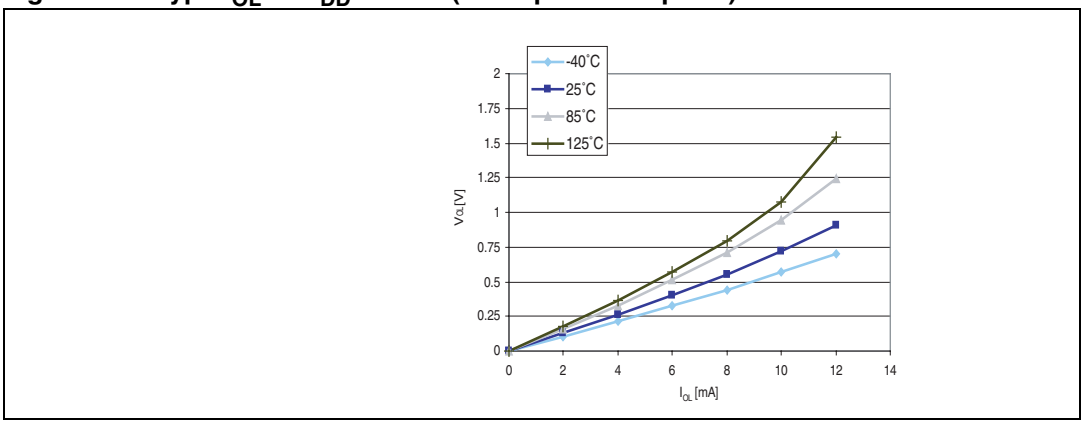


Figure 26. Typ. V_{OL} @ V_{DD} = 5 V (true open drain ports)

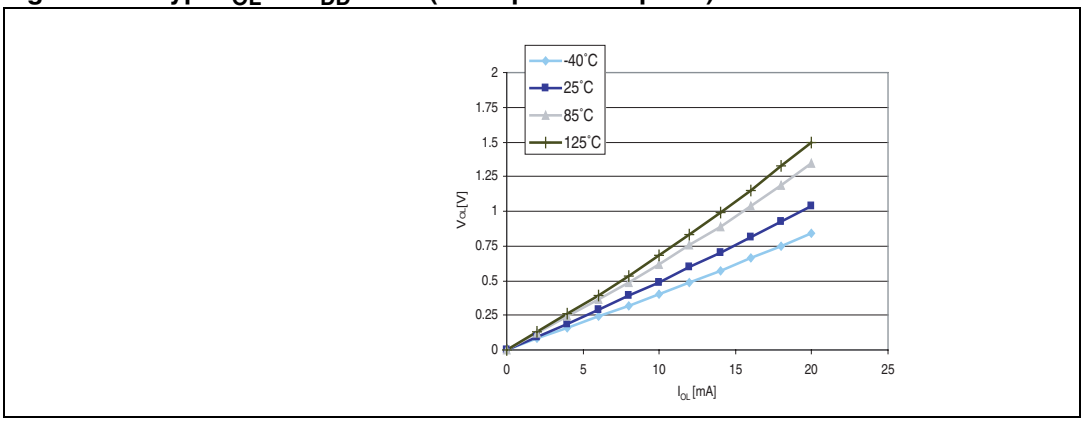


Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

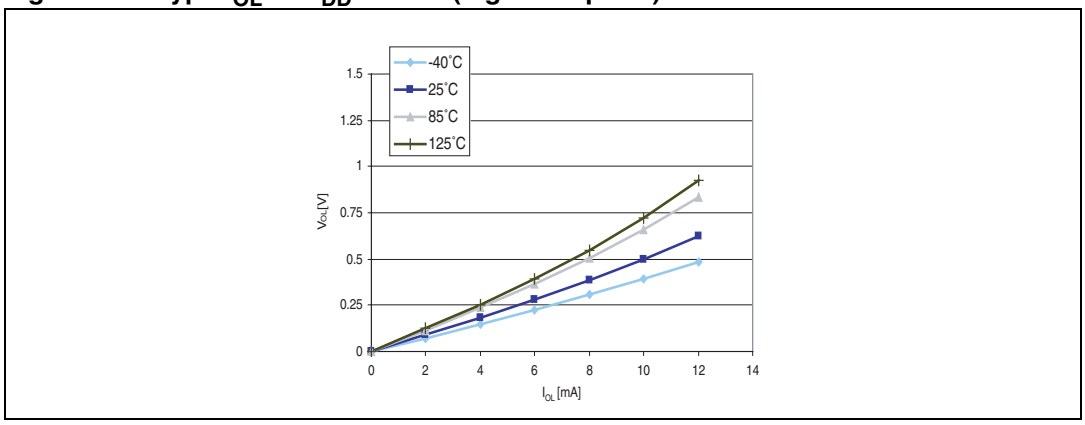


Figure 28. Typ. V_{OL} @ V_{DD} = 5 V (high sink ports)

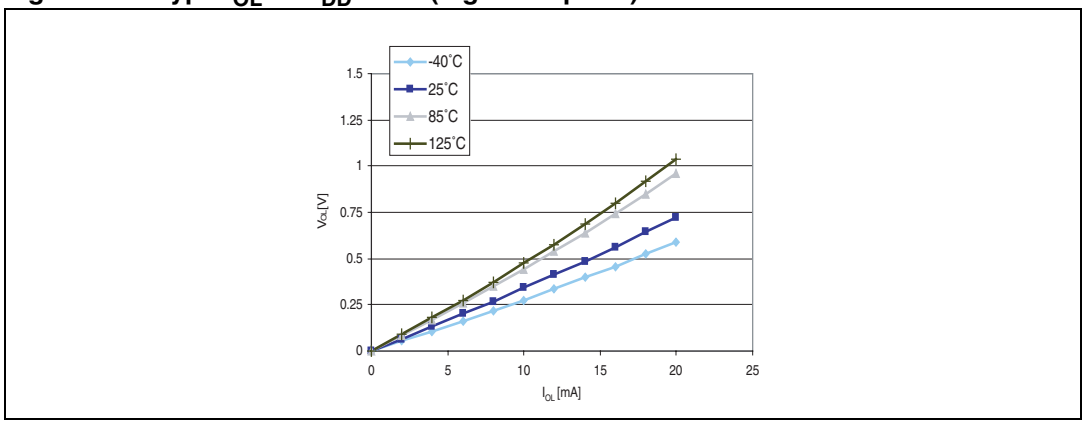


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

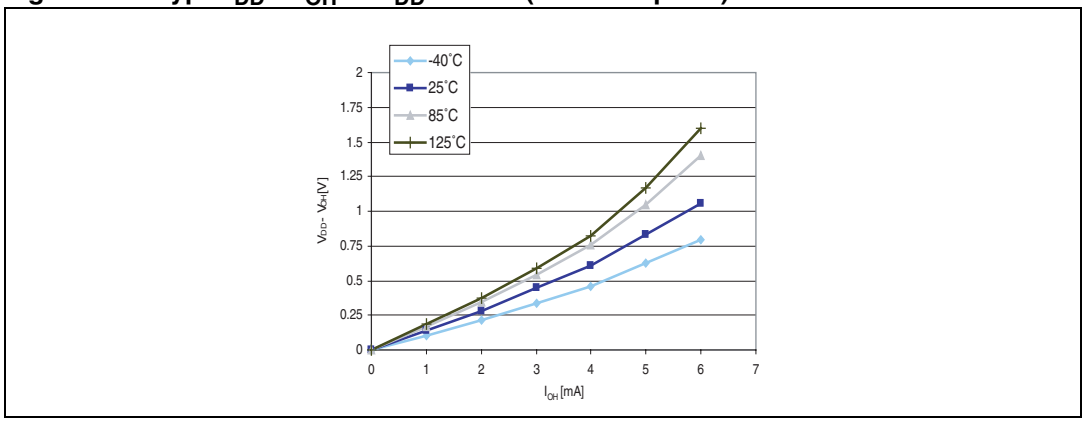


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports)

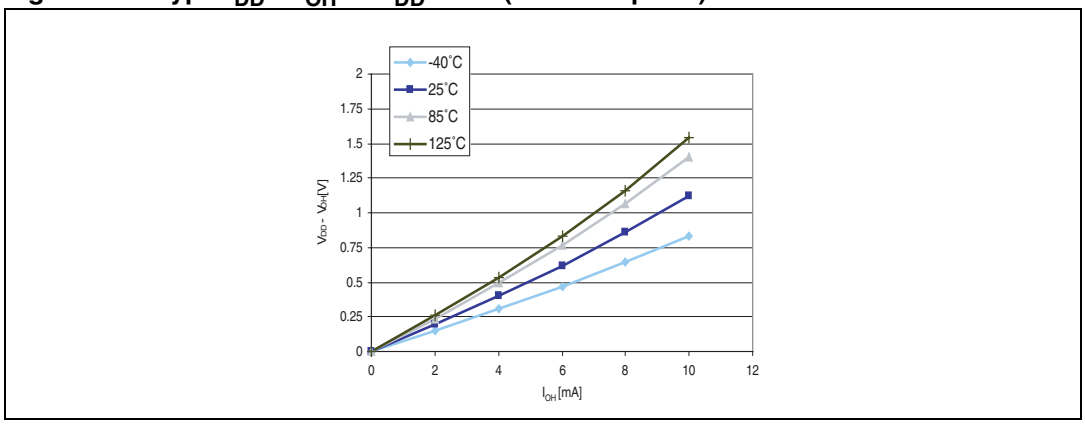


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

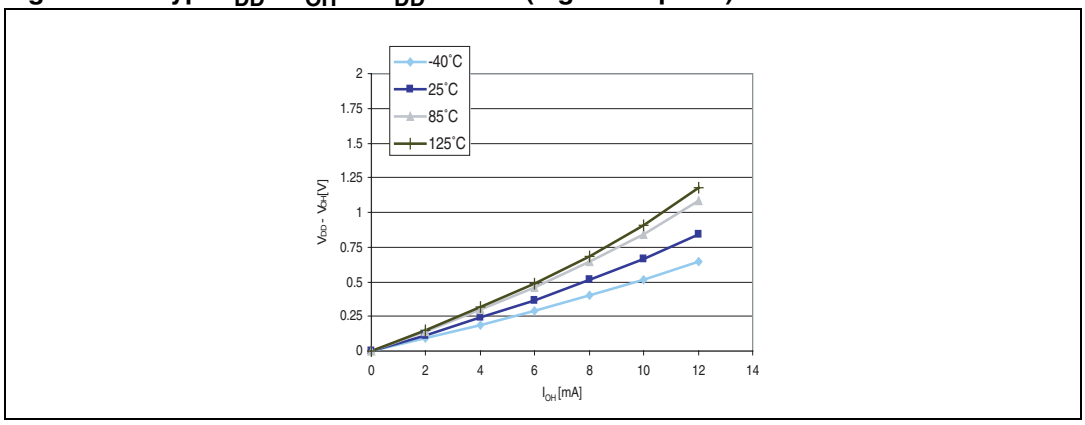
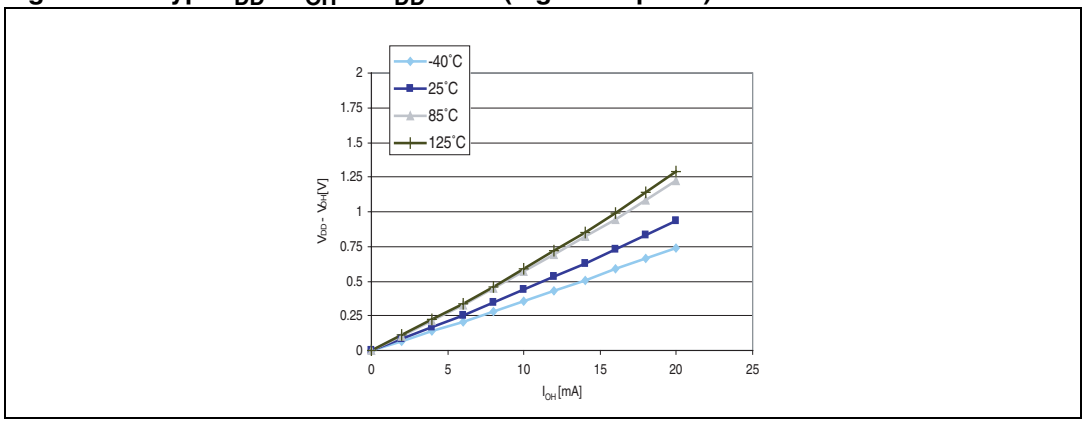


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports)



9.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 40. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage (1)		-0.3 V		0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage (1)		0.7 x V_{DD}		V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST Output low level voltage (1)	I_{OL}=2 mA			0.5	
$R_{PU(NRST)}$	NRST Pull-up resistor (2)		30	40	60	kΩ
$t_{IFP(NRST)}$	NRST Input filtered pulse (3)				75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse (3)		500			ns
$t_{OP(NRST)}$	NRST output pulse (3)		20			µs

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
3. Data guaranteed by design, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures

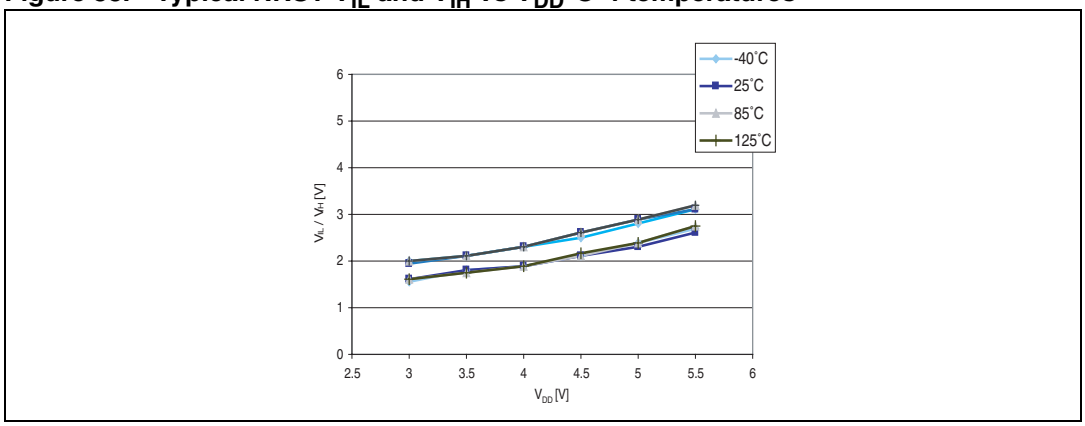


Figure 34. Typical NRST pull-up resistance vs V_{DD} @ 4 temperatures

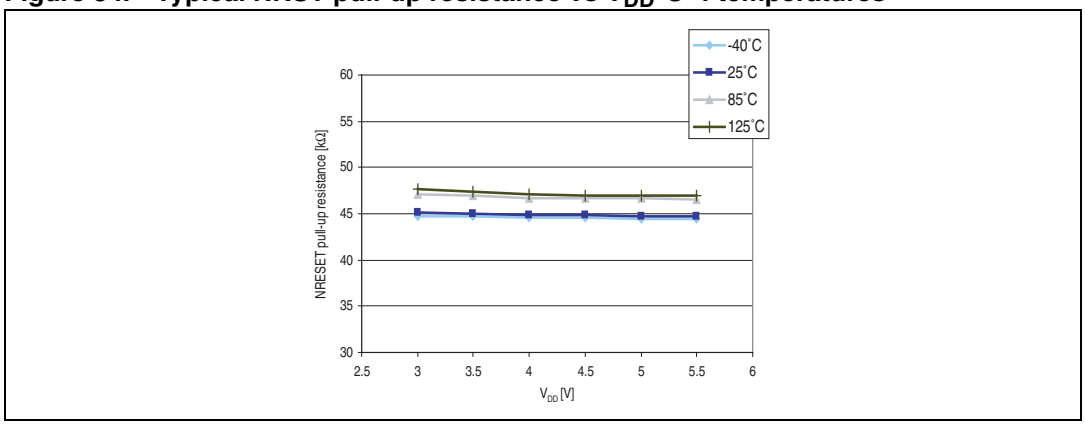
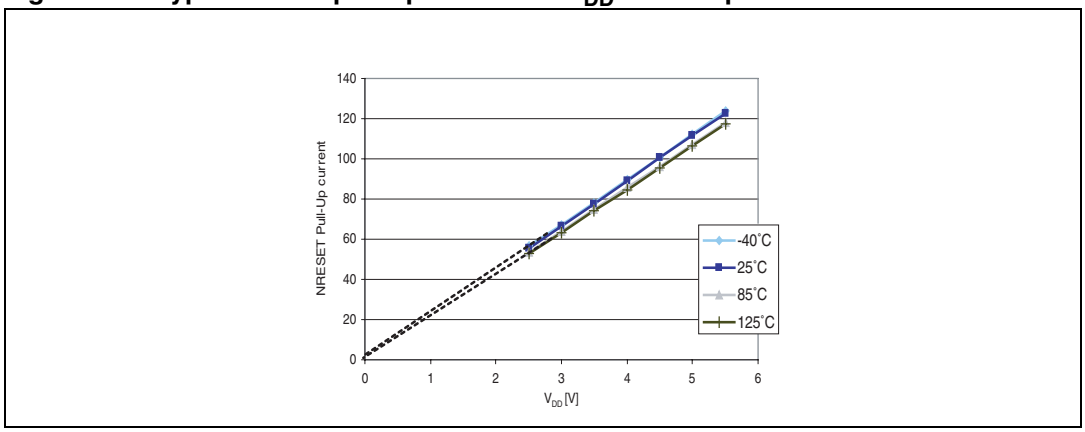
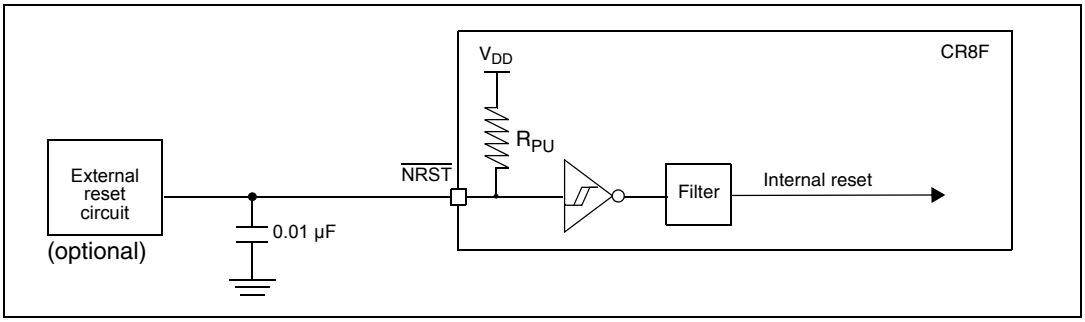


Figure 35. Typical NRST pull-up current vs V_{DD} @ 4 temperatures



The reset network shown in *Figure 36* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 36*. Otherwise the reset is not taken into account internally.

Figure 36. Recommended reset pin protection



9.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	TBD(2)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode	4 x t_{MASTER}		
$t_{h(NSS)}$(3)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode	$t_{SCK}/2$ - 15	$t_{SCK}/2$ +15	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode	5		
		Slave mode	5		
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode	7		
		Slave mode	10		
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		3 x t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode	25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)		TBD(2)	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)	27(2)		
$t_{h(MO)}$(3)		Master mode (after enable edge)	11(2)		

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Data characterization in progress.
3. Values based on design simulation and/or characterization results, and not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram - slave mode and CPHA = 0

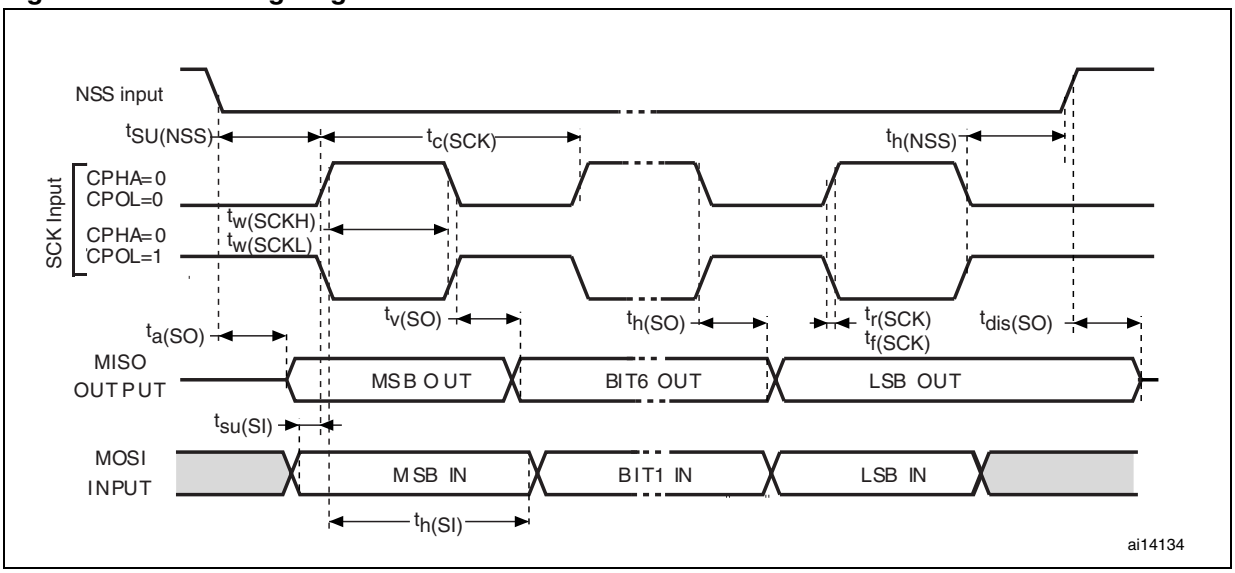
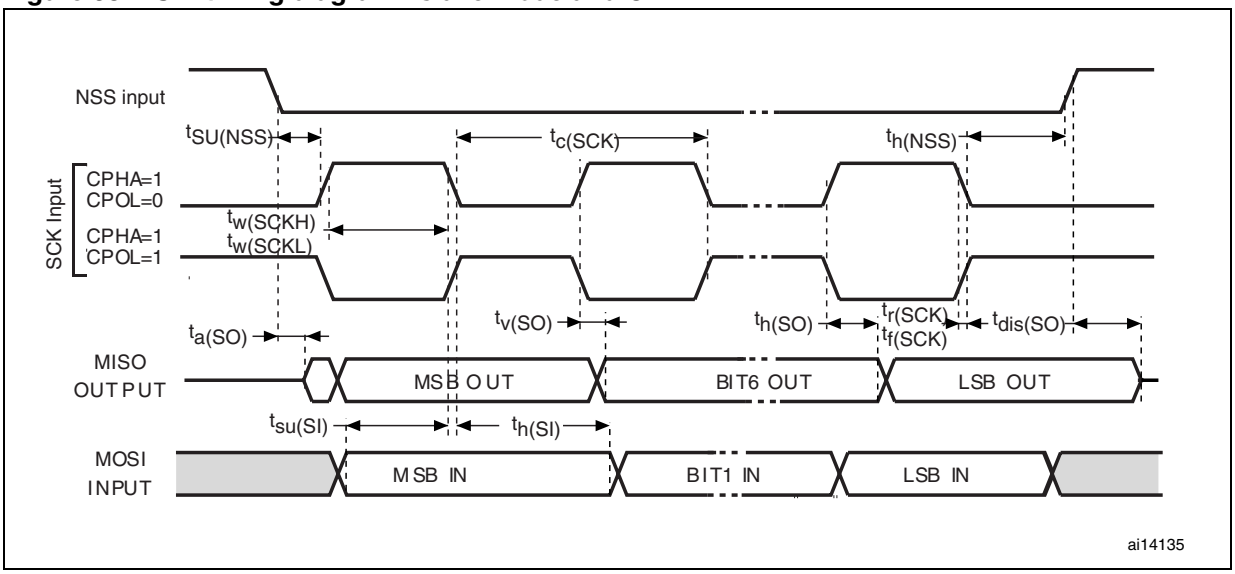
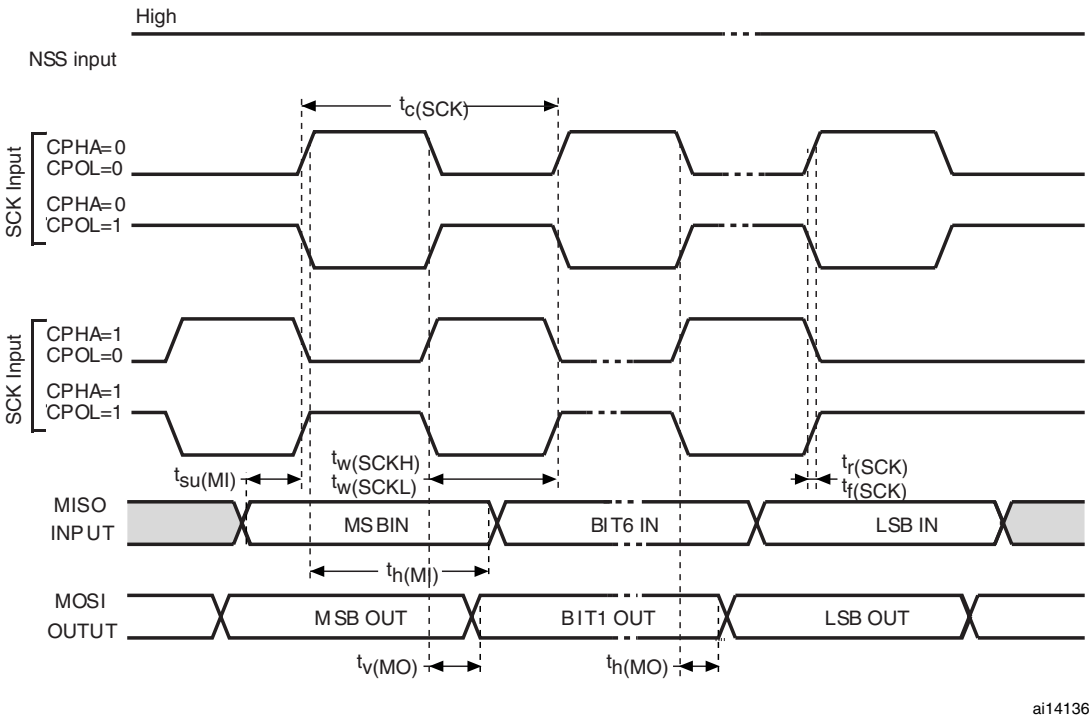


Figure 38. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7\ V_{DD}$.

Figure 39. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7\ V_{DD}$.

9.3.9 I²C interface characteristics

Table 42. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

9.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DD} = 2.95 to 5.5 V	1		**4**	MHz
		V_{DD} = 4.5 to 5.5 V	1		**6**	
V_{AIN}	Conversion voltage range(1)		V_{SS}		V_{DD}	V
V_{BGREF}	Internal bandgap reference voltage	V_{DD} = 2.95 to 5.5 V	1.19	1.22	1.25	V
C_{ADC}	Internal sample and hold capacitor			3		pF
t_S(1)	Minimum sampling time	f_{ADC} = 4 MHz		0.75		µs
		f_{ADC} = 6 MHz		0.5		
t_{STAB}	Wake-up time from standby			7		µs
t_{CONV}	Minimum total conversion time (including sampling time, 10-bit resolution)	f_{ADC} = 4 MHz	3.5			µs
		f_{ADC} = 6 MHz	2.33			µs
			14			$1/f_{ADC}$

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 44. ADC accuracy with R_{AIN} < 10 kΩ , V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error (2)	f_{ADC} = 2 MHz	1.6	TBD	LSB
		f_{ADC} = 4 MHz	2.2	TBD	
		f_{ADC} = 6 MHz	2.4	TBD	
$\|E_O\|$	Offset error (2)	f_{ADC} = 2 MHz	1.1	TBD	
		f_{ADC} = 4 MHz	1.5	TBD	
		f_{ADC} = 6 MHz	1.8	TBD	
$\|E_G\|$	Gain error (2)	f_{ADC} = 2 MHz	1.5	TBD	
		f_{ADC} = 4 MHz	2.1	TBD	
		f_{ADC} = 6 MHz	2.2	TBD	
$\|E_D\|$	Differential linearity error (2)	f_{ADC} = 2 MHz	0.7	TBD	
		f_{ADC} = 4 MHz	0.7	TBD	
		f_{ADC} = 6 MHz	0.7	TBD	
$\|E_L\|$	Integral linearity error (2)	f_{ADC} = 2 MHz	0.6	TBD	
		f_{ADC} = 4 MHz	0.8	TBD	
		f_{ADC} = 6 MHz	0.8	TBD	

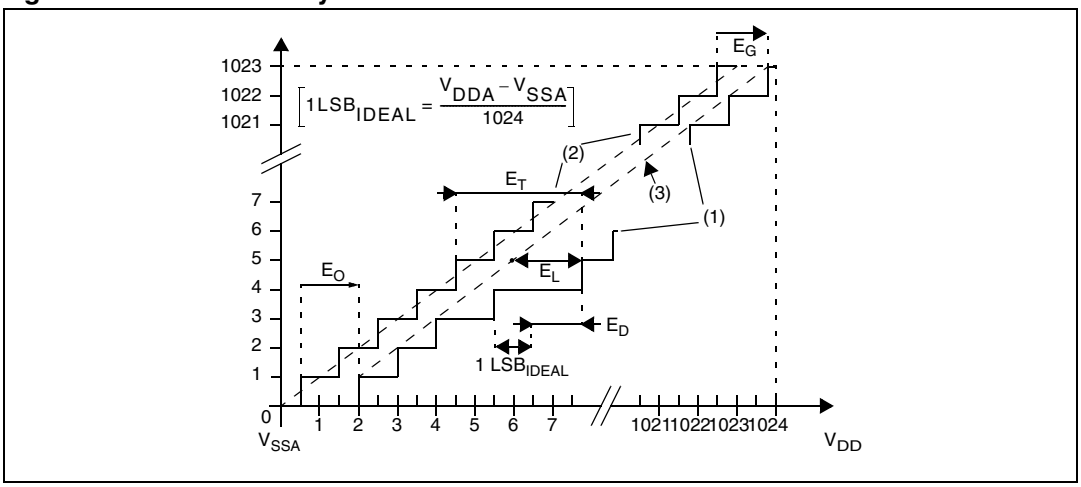
1. Data characterization in progress.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Table 45. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	TBD	LSB
		f_{ADC} = 4 MHz	1.9	TBD	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	1	TBD	
		f_{ADC} = 4 MHz	1.5	TBD	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	1.3	TBD	
		f_{ADC} = 4 MHz	2	TBD	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	TBD	
		f_{ADC} = 4 MHz	0.7	TBD	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	TBD	
		f_{ADC} = 4 MHz	0.8	TBD	

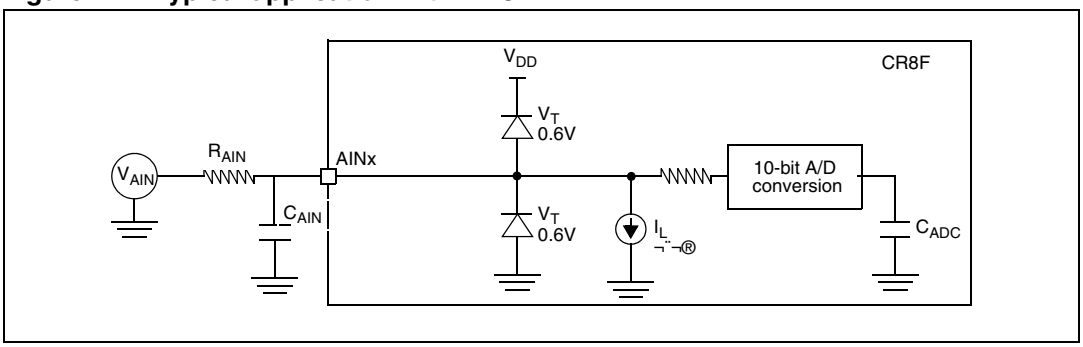
1. Data characterization in progress.

Figure 40. ADC accuracy characteristics



1. Example of an actual transfer curve.
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: deviation between the first actual transition and the first ideal one.
   E_G = Gain error: deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Figure 41. Typical application with ADC



9.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 46. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{MASTER} = 16 MHz (HSI clock), conforming to IEC 1000-4-2	2/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A = 25 °C , f_{MASTER} = 16 MHz (HSI clock), conforming to IEC 1000-4-4	4/A

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 47. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{HSE}/f_{CPU}(1)		
				16 MHz/ 8 MHz	16 MHz/ 16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V T_A = 25 °C LQFP32 package Conforming to SAE J 1752/3	0.1MHz to 30 MHz	2	3	dBµV
			30 MHz to 130 MHz	10	10	
			130 MHz to 1 GHz	5	7	
	SAE EMI level		SAE EMI level	2.5	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU, and DLU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 48. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A LQFP32 package = 25°C, conforming to SD22-C101	IV	1000	

1. Data based on characterization results, not tested in production

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 49. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	A
		T_A = 125 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

10 Package characteristics

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*. ECOPACK® is an ST trademark.

10.1 Package mechanical data

10.1.1 LQFP package mechanical data

Figure 42. 32-pin low profile quad flat package (7 x 7)

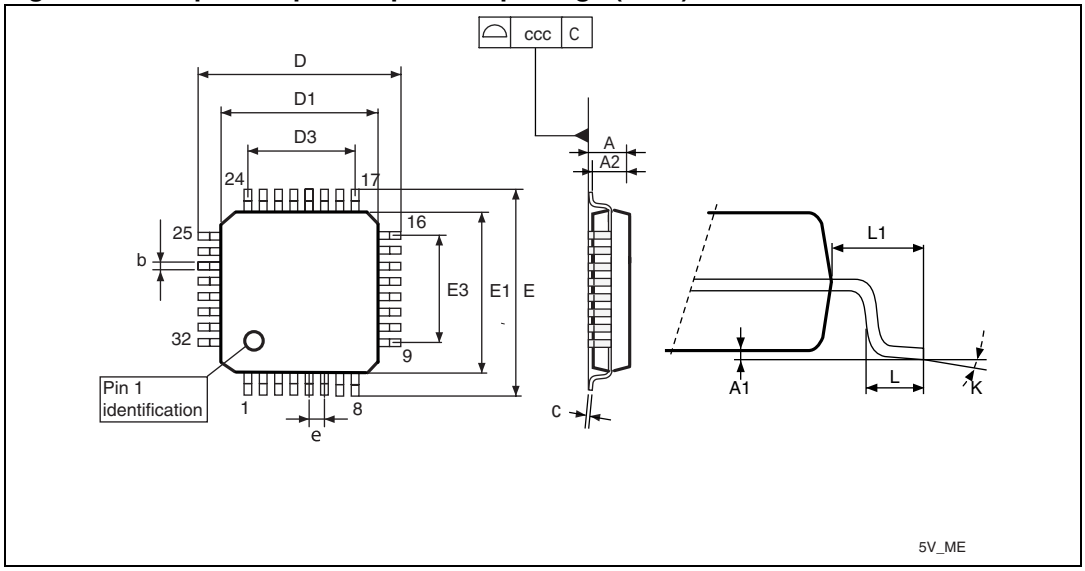


Table 50. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc			0.100			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits

10.1.2 VFQFPN package mechanical data

Figure 43. 32-lead very thin fine pitch quad flat no-lead package (5 x 5)

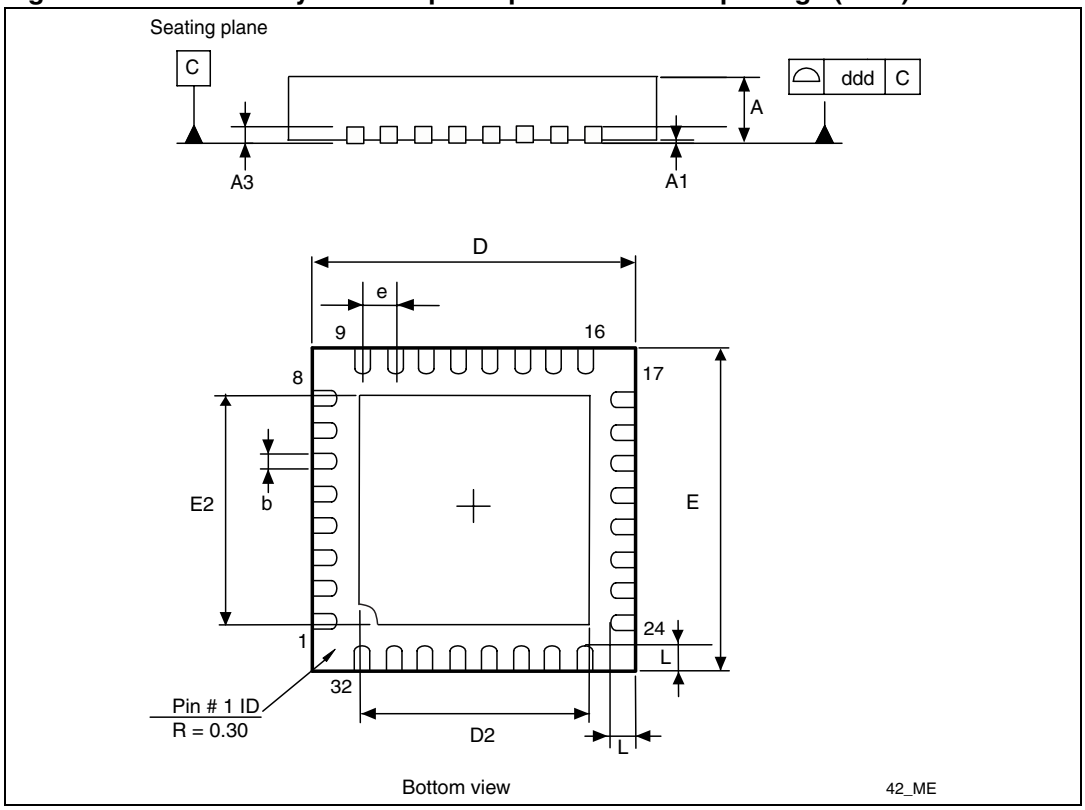
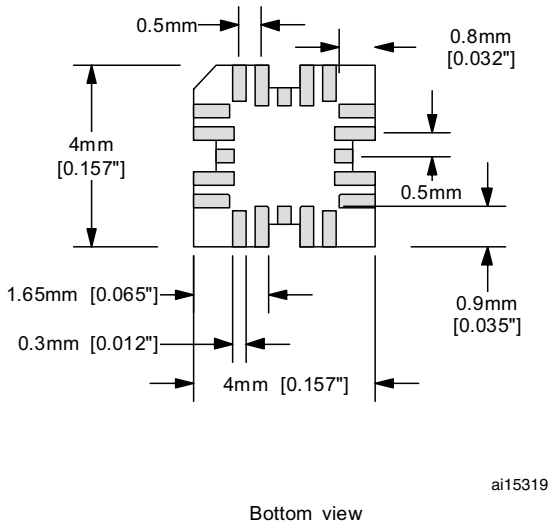


Table 51. 32-lead very thin fine pitch quad flat no-lead package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
D2	3.20	3.45	3.70	0.1260		0.1457
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
E2	3.20	3.45	3.70	0.1260	0.1358	0.1457
e		0.50			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd			0.08			0.0031

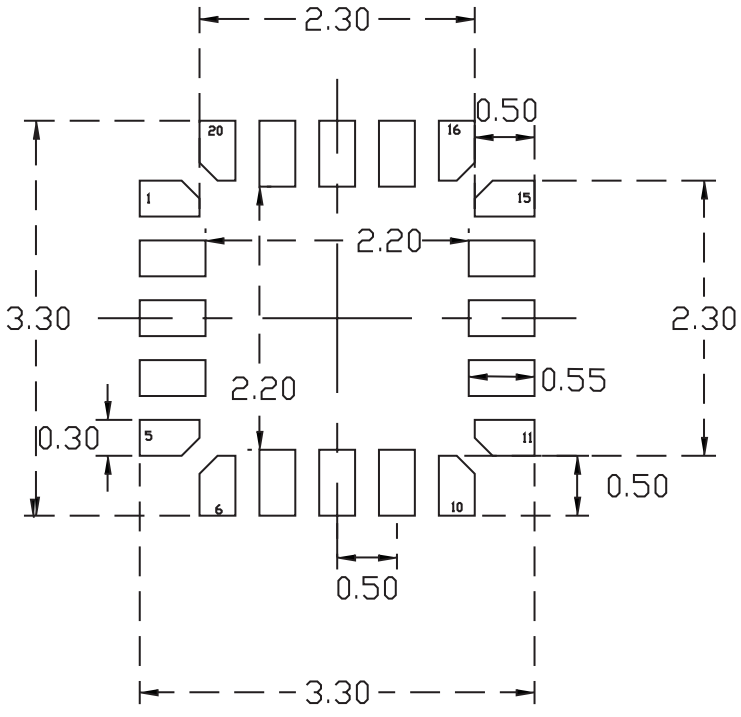
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. Recommended footprint for on-board emulation



1. Drawing is not to scale

Figure 45. Recommended footprint without on-board emulation



1. Drawing is not to scale
2. Dimensions are in millimeters

10.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 17: General operating conditions on page 44*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($PDmax = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 52. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W
Θ_{JA3}	Thermal resistance junction-ambient VFQFPN 32 - 5 x 5 mm	22	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.2.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

10.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 11: Ordering information on page 84*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature T_{Amax}= 75 °C (measured according to JESD51-2)
- I_{DDmax} = 8 mA, V_{DD} = 5 V
- Maximum 20 I/Os used at the same time in output at low level with
  I_{OL} = 8 mA, V_{OL}= 0.4 V
  P_{INTmax} = 8 mA x 5 V = 400 mW
  P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW
  This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:
  P_{Dmax} = 400 mW + 64 mW
  Thus: P_{Dmax} = 464 mW

Using the values obtained in *Table 52: Thermal characteristics on page 82*, T_{Jmax} is calculated as follows for LQFP32 59°C/W:

T_{Jmax} = 75° C + (59° C/W x 464 mW) = 75°C + 27°C = 102° C

This is within the range of the suffix 6 version parts (-40 < T_J < 105° C).

In this case, parts must be ordered at least with the temperature range suffix 6.

12 CR8F development tools

Development tools for the CR8F microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the CR8F is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, CR8F application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of CR8F microcontrollers via the CR8F single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for CR8F.

12.2 Software tools

CR8F development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for CR8F, which are available in a free version that outputs up to 16 Kbytes of code.

12.2.1 CR8F toolset

CR8F toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST visual develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your CR8F microcontroller's Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for CR8F*** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for CR8F*** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.raisonance.com.
- ***CR8F assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows you to assemble and link your application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the CR8F Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your CR8F.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the CR8F family.

13 Revision history

Table 53. Document revision history

Date	Revision	Changes
30-Apr-2009	1	Initial revision

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